Riccar / TEAL Calculator

Contents

This schematic has been derived through reverse engineering.
This is not the manufacturer's schematic, nor based on the manufacturer's schematic.

Notes

- The symbol Ncp denotes a physical connector pin, where *c*=connector and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- The symbol ▲ without an additional label denotes VDD (–24V).
- Capacitance in microfarads unless otherwise indicated.
- IC identifiers have been created for this drawing and may not correspond to labels on the boards.
- This drawing is based on observation of board photographs of one unit.
  Photographs, tracings of hidden tracks and measurements supplied by Jef Ongena of Belgium.

Log

• 2021 Feb	Initial drawing, timing and display sections only / bhilpert.
• 2021 Apr-May	Remaining sections added / bh.
• 2021 Jun-Aug	Minor revisions / bh.

Logic Presentation

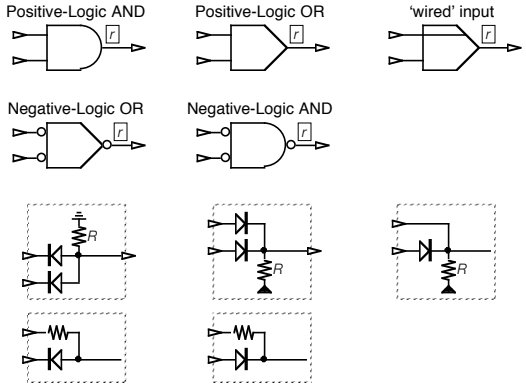
Gate symbols and signal names are presented in accordance with:
logic 1 = GND
logic 0 = V–24

The design uses primarily negative logic in the control portion and positive logic for data and registers.

Logic Implementation

The logic is implemented with a combination of early SSI and MSI MOS integrated circuits from the JMOS family, and discrete DTL. Most gates are constructed from discrete diodes and resistors. Inverters, active gates, flip-flops and more complex logic elements are contained in the integrated circuits. The active elements are open-drain outputs, closing to GND (logic 1), requiring external pull-down resistors to –24V (logic 0).

The internal construction of discrete gates is shown in the following diagrams. A wire–OR or wire–AND construction is indicated by the input line traversing the width of the gate. The design is heavily optimised for component reduction with many gates having one input formed from the pull-up/down load resistor, rather than a diode and fixed-supply resistor.



The diodes may be individual components or contained in 4-diode TSxxx modules. Gate inputs are identified either by a pin number in the case of a diode in a module, the ID of the discrete diode forming the input, or the R value in the case of a resistor.

For gates with fixed-supply load resistors (*R*), to reduce clutter, the resistors are indicated in the schematic by one of the following letters (*r*) in a box by the output.

Symbol (*r*)	Resistance (*R*)
3	30K to VDD
5	50K to VDD
1	100K to VDD
30	300K to VDD

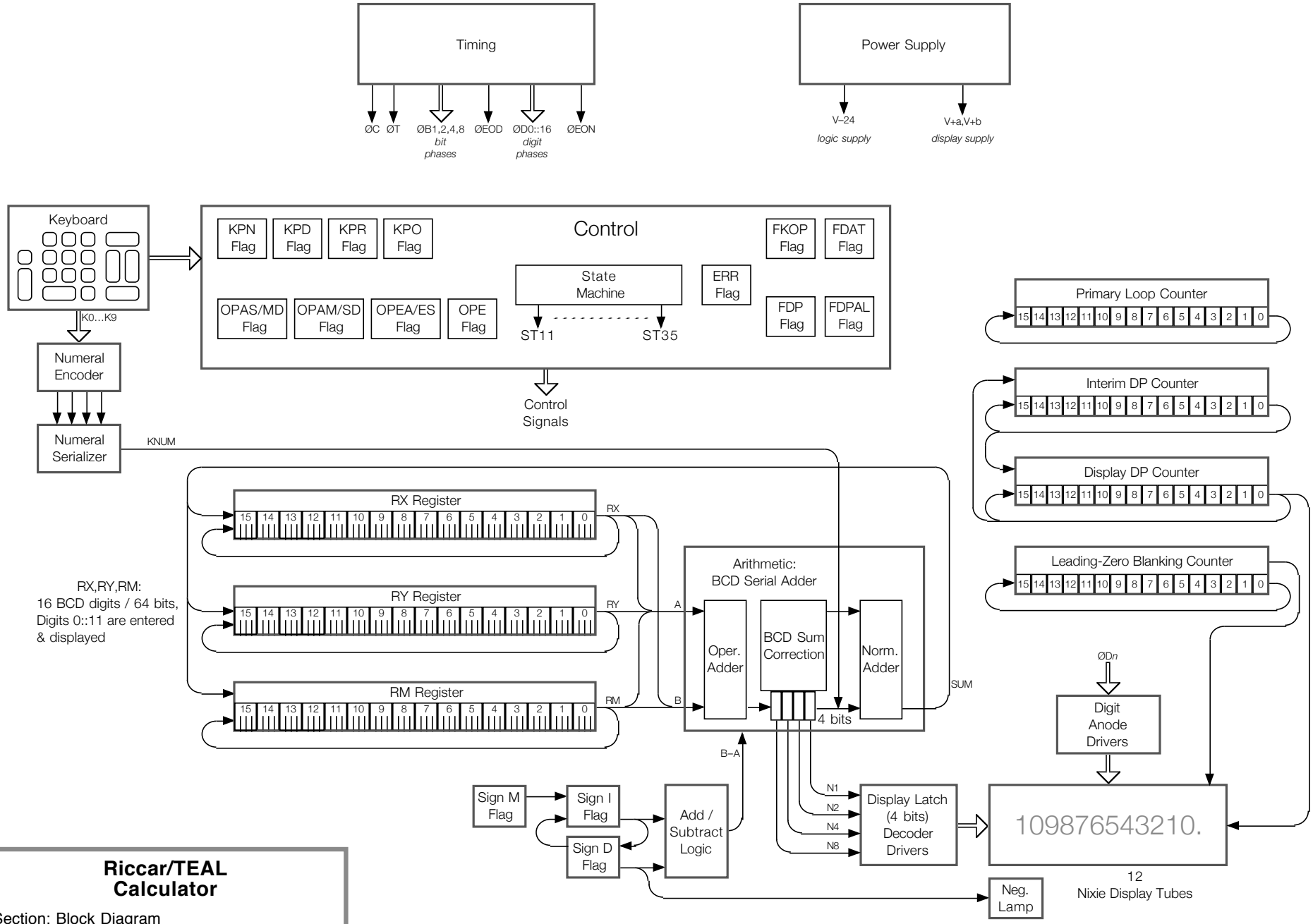
Symbol (*r*)	Resistance (*R*)
a	100K to GND
b	200K to GND
c	10K to GND
d	30K to GND
e	300K to GND

Clocking Scheme

The flip-flops in the JMOS logic family are a form of Master/Slave D-type flip-flop with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while outputs are changed synchronously by a single clock signal.

ØC = Capture Input (master section clock)
ØT = Transition Input (slave section clock)

The state of the D input is captured when ØC is logic 0 (–24V). The Q output is set in accordance with the captured state when ØT goes to logic 0.



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Section: Block Diagram
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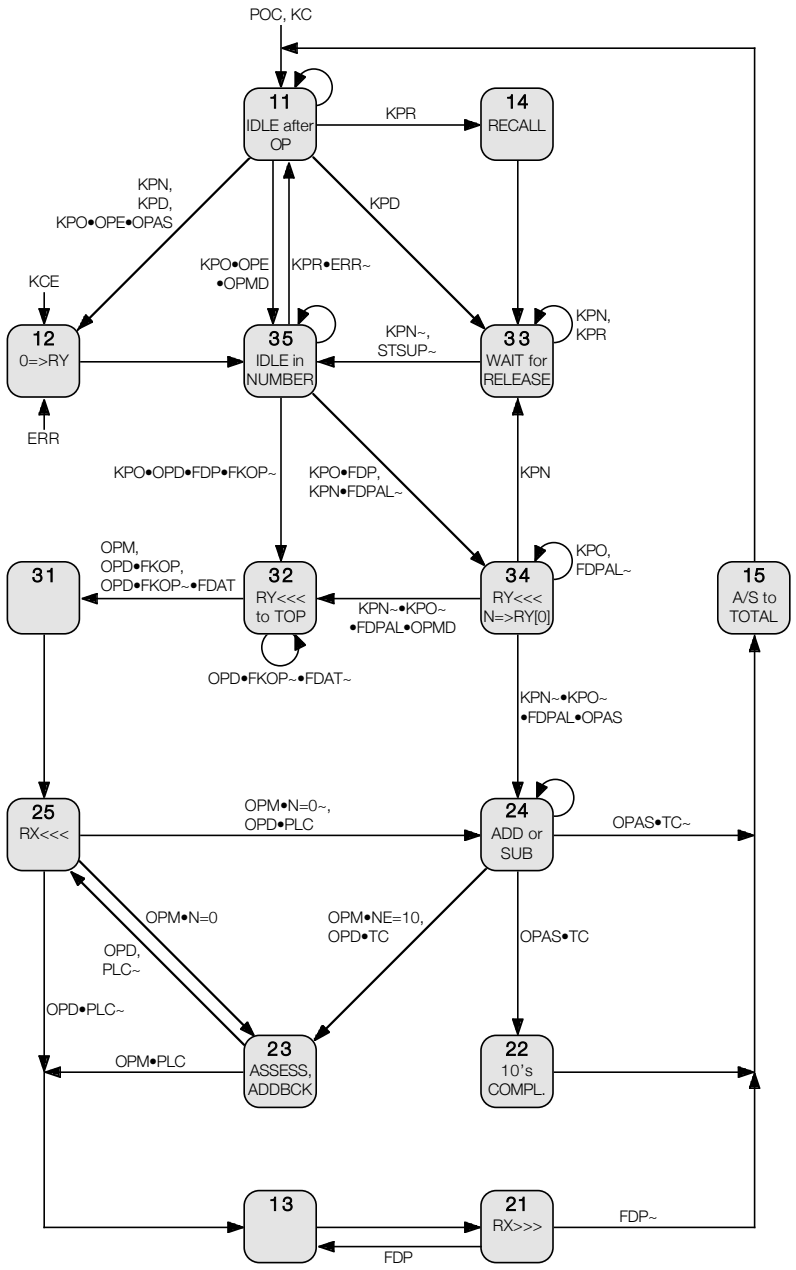
State Actions

DEFAULT:			RX=>B	S=>RX	RY=>RY	RM=>RM
POC:	Power-On-Clear	0=>RM	0=>SNM	1=>OPAS,OPAM	KC	
KC:	Clear	0=>RX	0=>SND,SNO	0=>ERR	1=>OPAS,OPAM? 0=>FKOP	
ST11:	Idle loop, RX displayed.	FKOP~:S=>RY				
ST12:	Prepare RY for number entry. Clear DPD Counter. Clear Zero-Blanking Counter.	RX=>RX	0=>RY	0=>SND	0=>FDP	1=>ST12DONE
ST13:	Clear remnant digits in RX, shift PLC.(?)					
ST14:	Copy RM to RY. Clear Zero-Blanking Counter.	RM=>A	0=>B	FKOP~:S=>RY	SNM => SND	
ST15:	Add or Subtract to Memory Register. Clear Zero-Blanking Counter.					
ST21:	Shift RX down.					
ST22:	RY complemented into RX.	RY=>A	0=>B	B–A=1	SNO~=>SNO	
ST23:	Division: add back to correct overdraft.(?)	OPD:RY=>A				
ST24:	Primary arithmetic state for A,S,M & D. M: loop till D15=?. D: loop till Tens Carry @ ØD0.	RY=>A TC~:9=>A[14]	OPAS:A=>RY	enable B–A logic	PLC: 1=>FDAT	
ST25:	Shift RX up. OPM: shift PLC up. OPD: shift PLC up if FDP~.					
ST31:	(?)	OPE:1=>FKOP SND?SNO	DPa=>DPD RX shift?	FKOP~:DPD=>DPa DPD shift?		
ST32:	Shift RY up till RY[12?] ≠ 0.	STRYLA: RX=>RX, RY=>A, S=>RY		0=>PLC[14]		
ST33:	Clear RM if Recall. Loop till KPN & KPR are released.	FKOP~:RX=>RX 0=>FDAT~	FKOP~:RY=>A 0=>RX (•OPE)	FKOP~:S=>RY	0=>RM (•KT•KPR)	
ST34:	DP Alignment to Setpoint. Shift DPD up until =ØDPS. Enter KNUM into bitstream (for KPN).	FKOP~:RX=>RX DPD no shift on ØD16	FKOP~:RY=>A	FKOP~:S=>RY	(RY clock alteration)	
ST35:	Idle loop for number entry, RY displayed.	0=>R[15] if no DP: DPD=0?	FKOPNT:RX=>RX,RY=>A,S=>RR2 SNO=0?		0Mark=>PLC[14]	

NOT COMPLETE

Note: In multiplication and division, the Primary Loop is 24 –> 23 –> 25. The Secondary Loop is the self-loop on 24.



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Section: State Diagram & Descriptions
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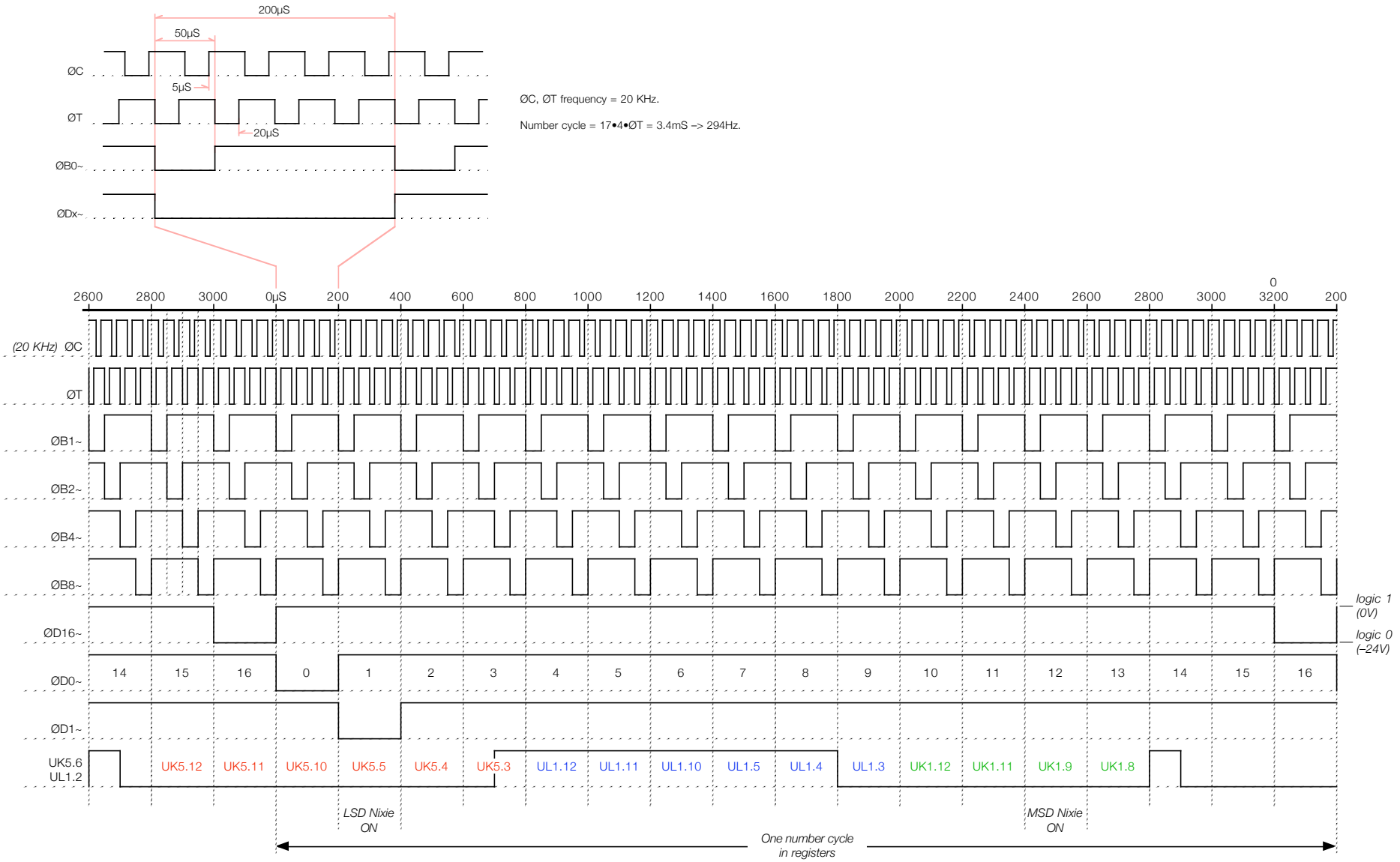
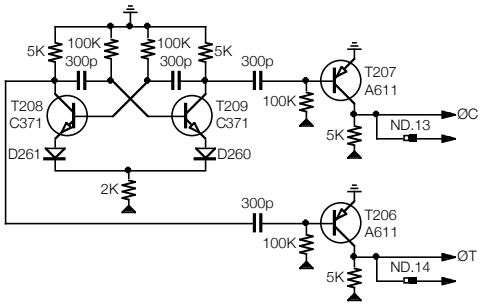
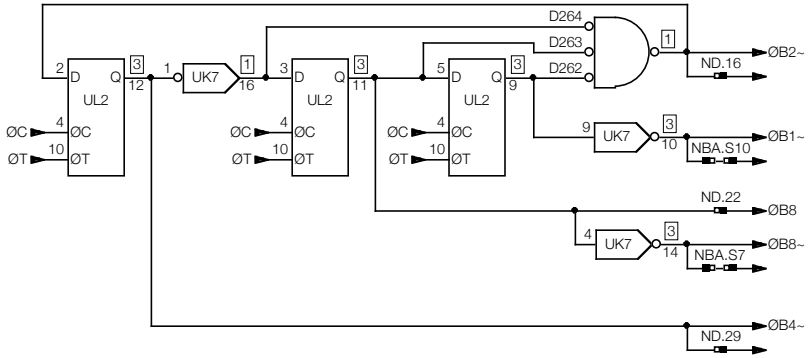

200µS
50µS
5µS
20µS
ØC
ØT
ØB0~
ØDx~
ØC, ØT frequency = 20 KHz.
Number cycle = 17•4•ØT = 3.4mS –> 294Hz.
2600 2800 3000 0µS 200 400 600 800 1000 1200 1400 1600 1800 2000 2200 2400 2600 2800 3000 0 3200 200
(20 KHz) ØC
ØT
ØB1~
ØB2~
ØB4~
ØB8~
ØD16~
ØD0~
ØD1~
UK5.6 UL1.2
14 15 16 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
UK5.12 UK5.11 UK5.10 UK5.5 UK5.4 UK5.3 UL1.12 UL1.11 UL1.10 UL1.5 UL1.4 UL1.3 UK1.12 UK1.11 UK1.9 UK1.8
logic 1 (0V)
logic 0 (–24V)
LSD Nixie ON
MSD Nixie ON
One number cycle in registers

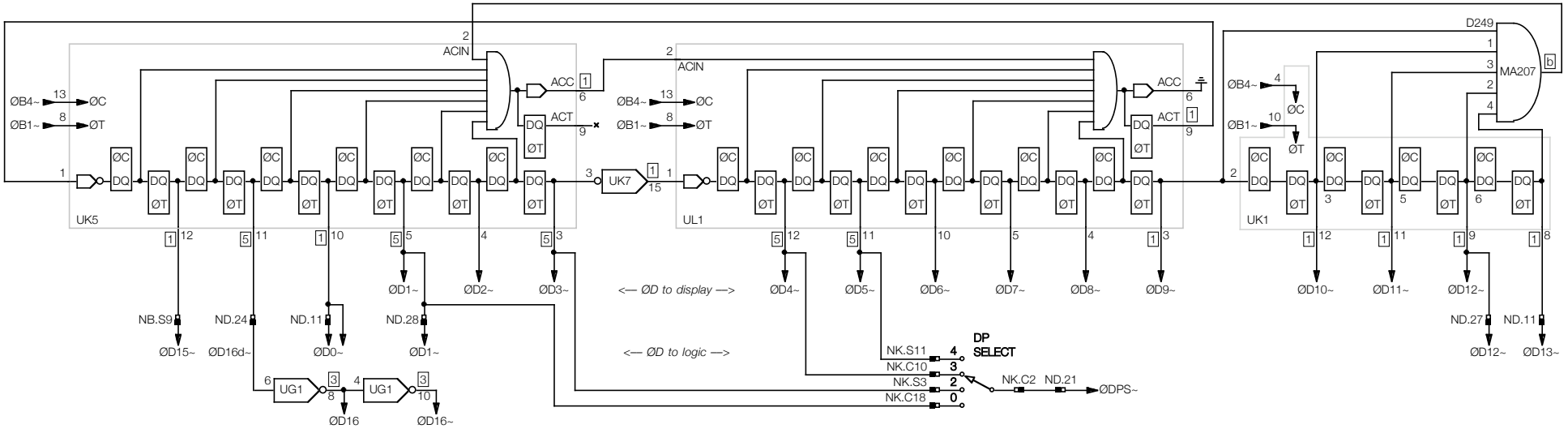
Master Clock

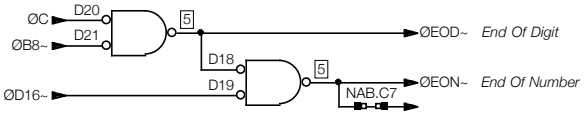


Bit Phases
Ring Counter



Digit Phases
Ring Counter





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Section: Timing
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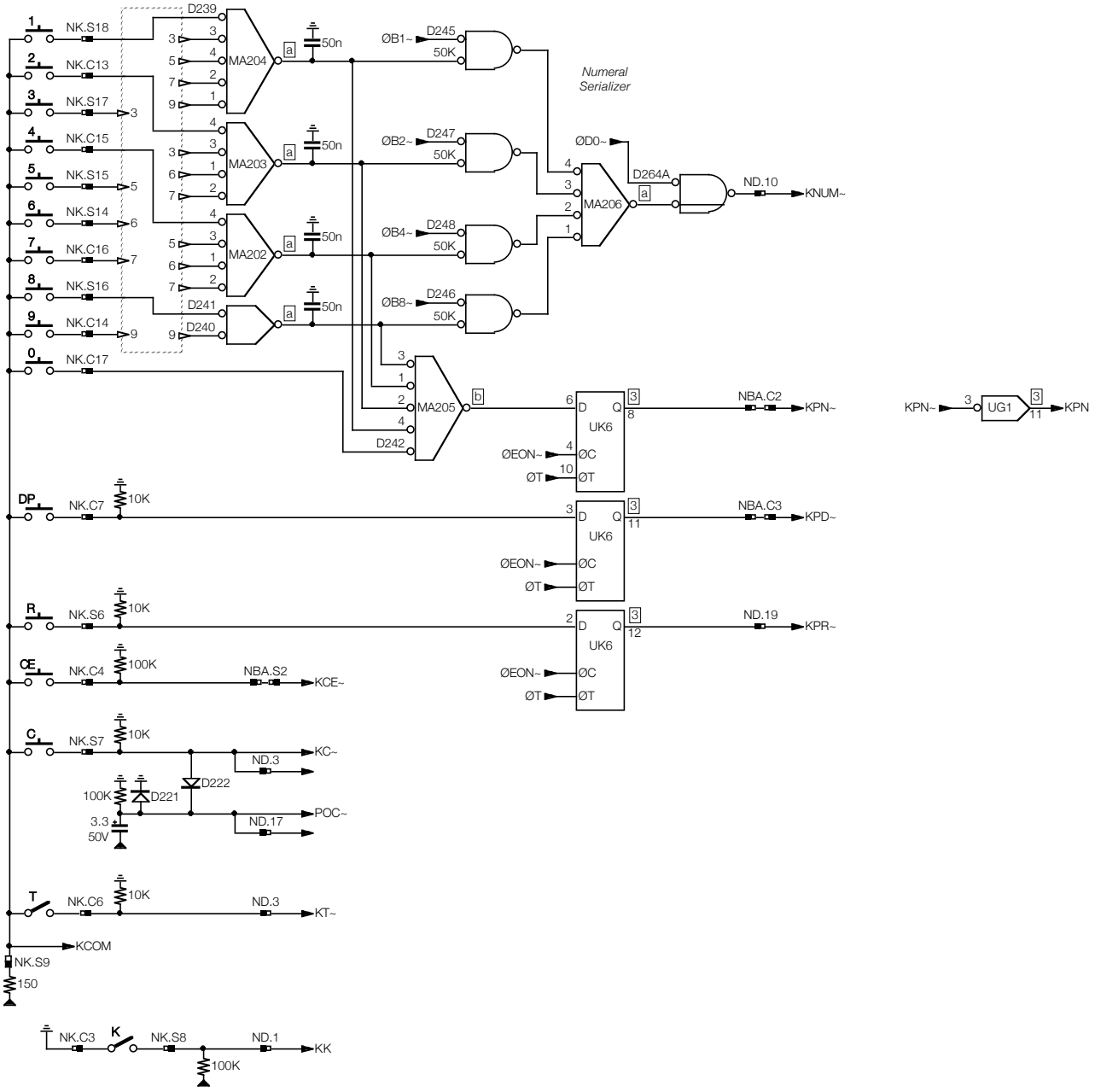

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Section: Keyboard - Numeral Encoding
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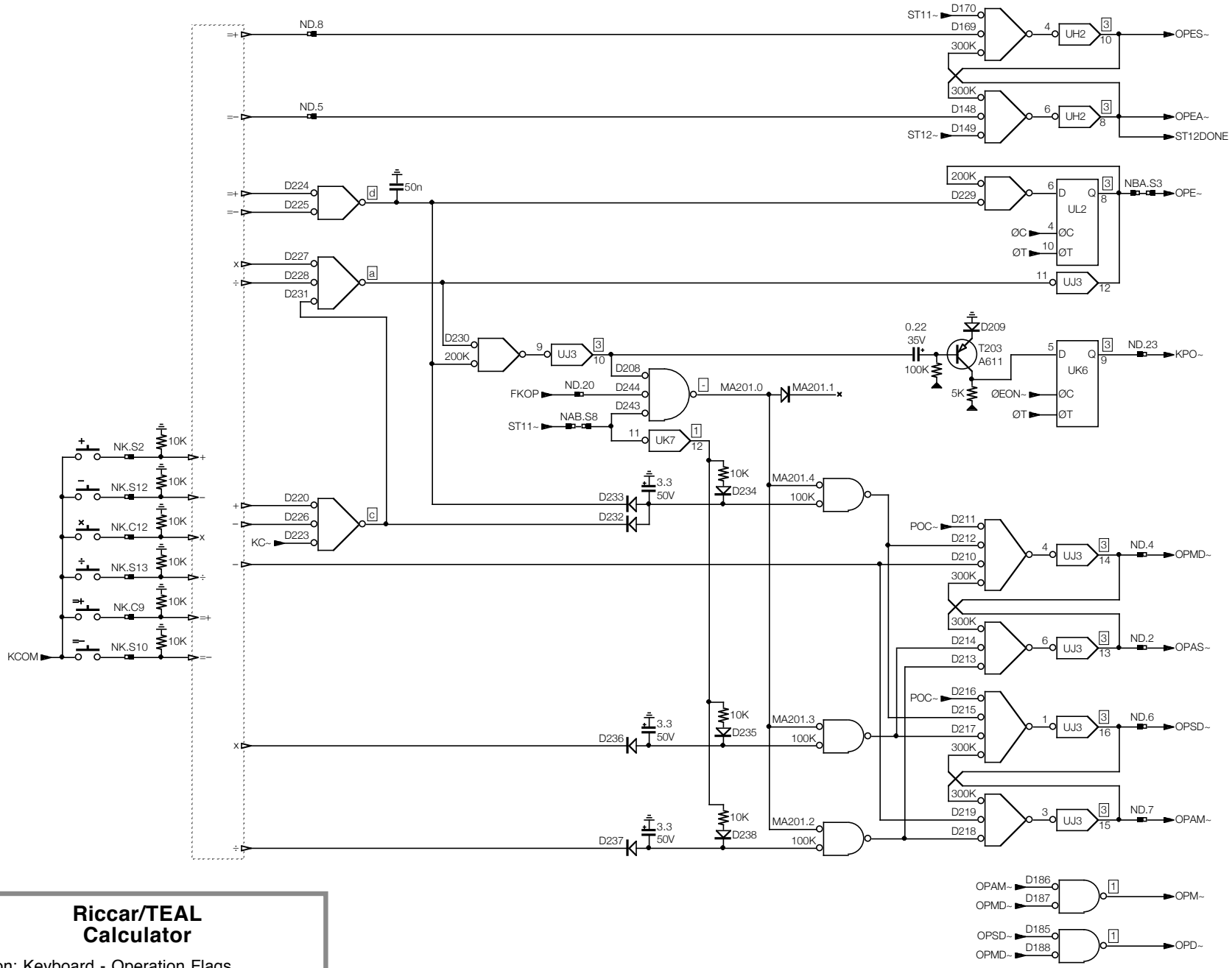

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Section: Keyboard - Operation Flags
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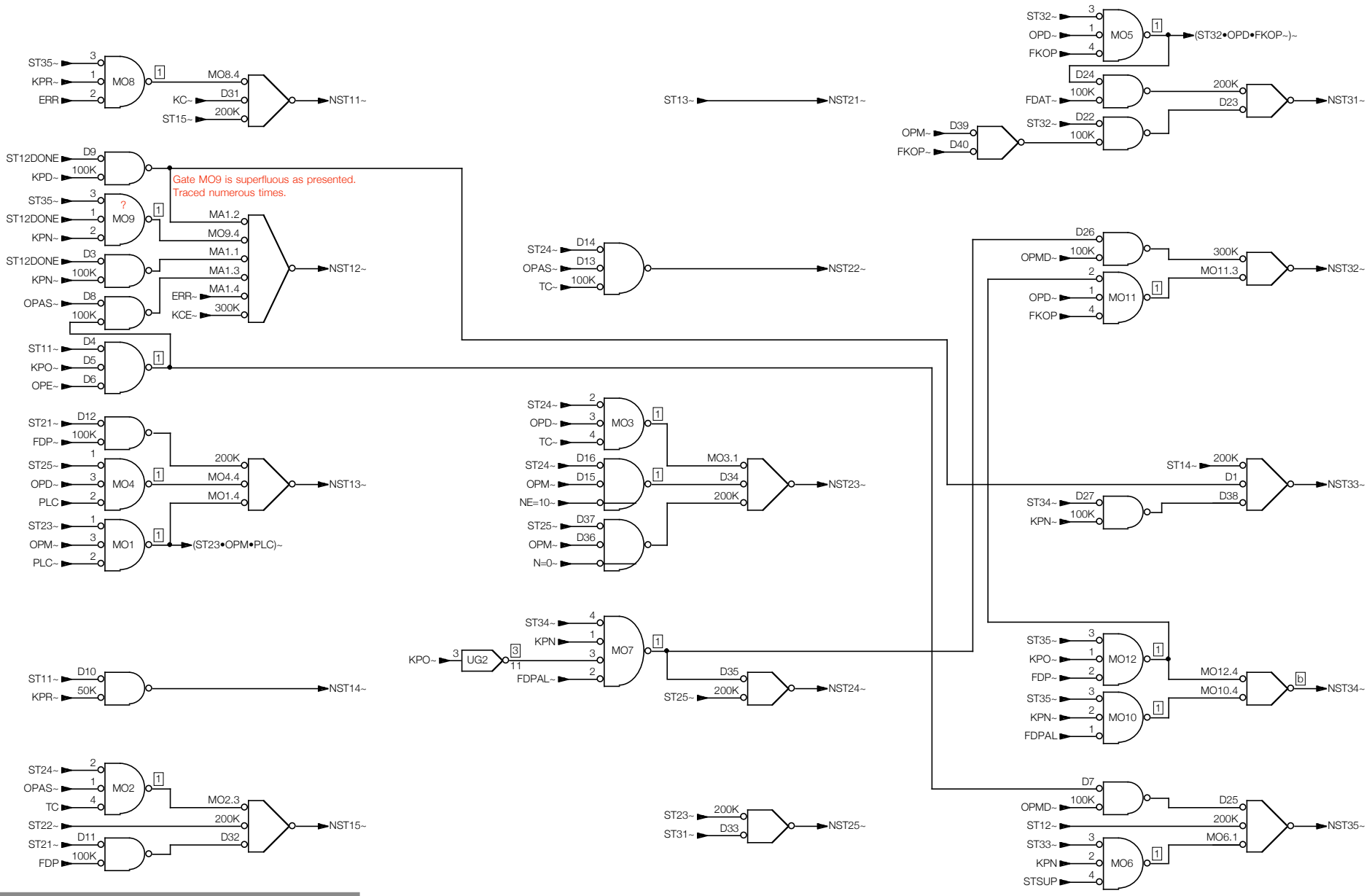

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Section: Control - Next State Logic

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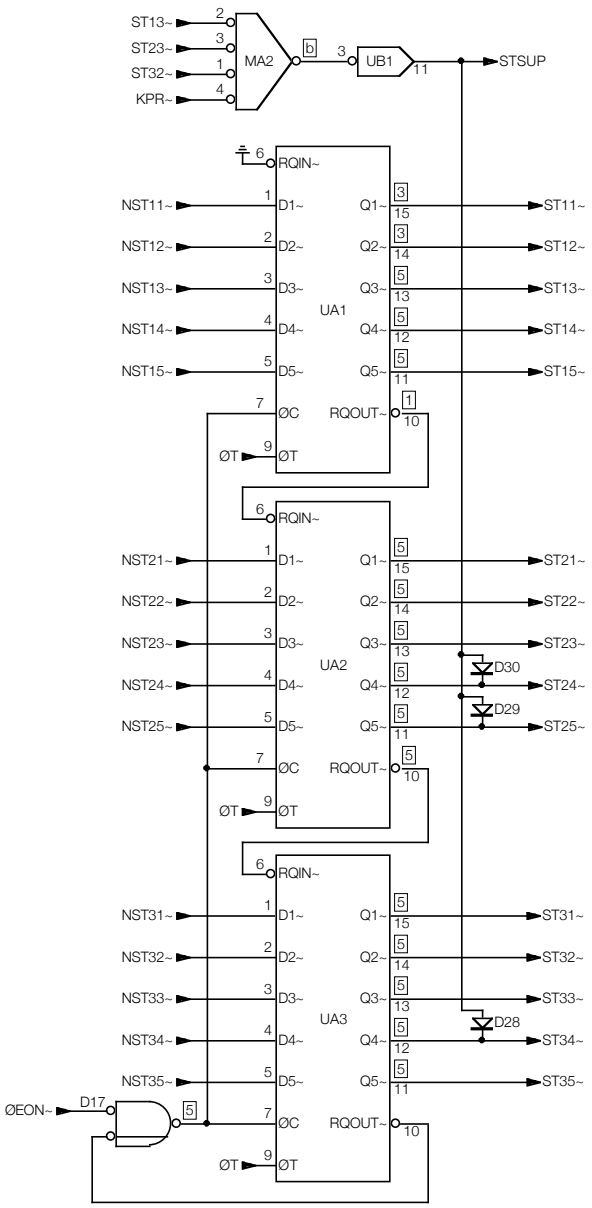
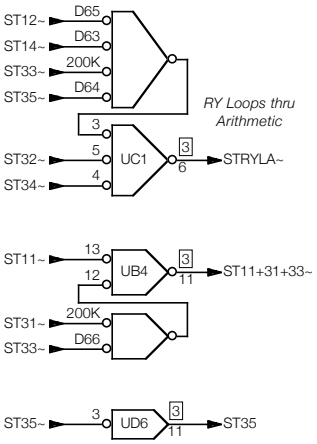
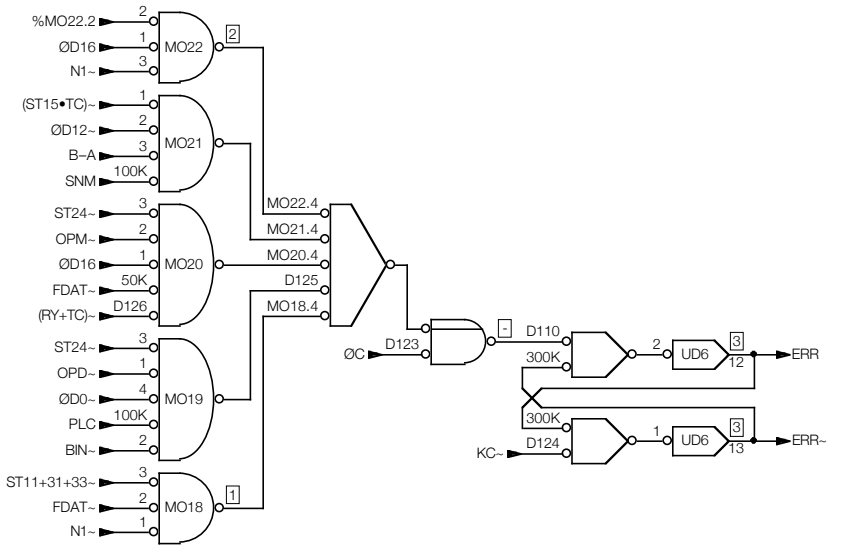


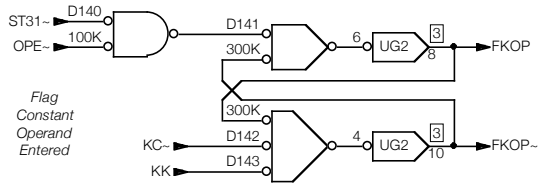
State Suppression:
- ST13 suppresses ST25
- ST13 suppresses ST24
- ST23 suppresses ST24
- ST32 suppresses ST24
- ST32 suppresses ST34

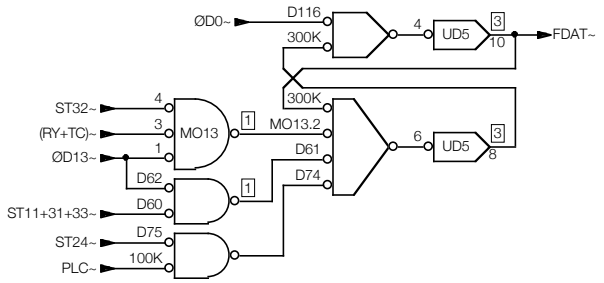
State 12 & 33 are asserted simultaneously during KPD.

State 12 & 35 are asserted simultaneously in error state.









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Section: Control - State Registers & Flags
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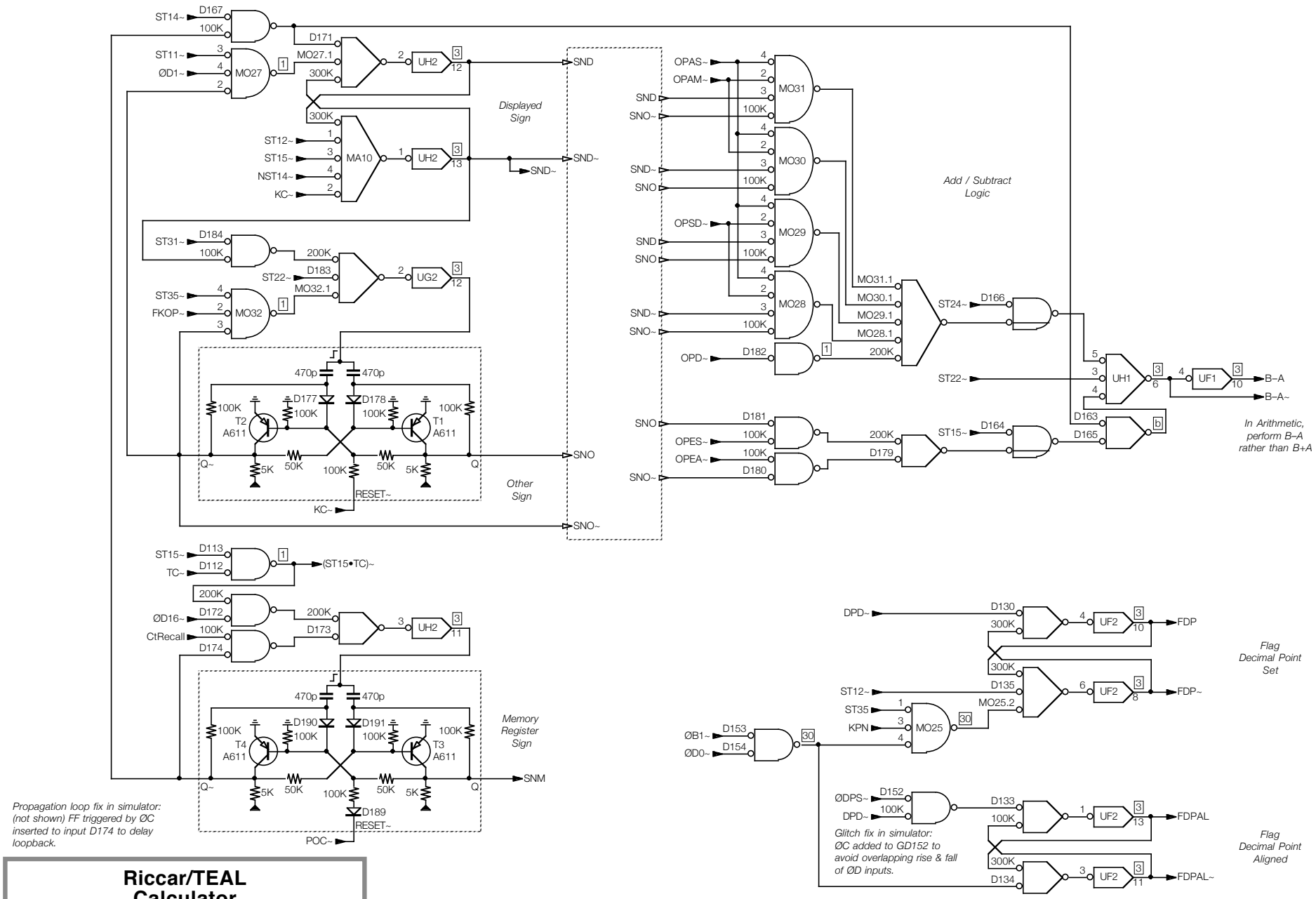

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Section: Sign Flags & A/S Logic, DP Flags
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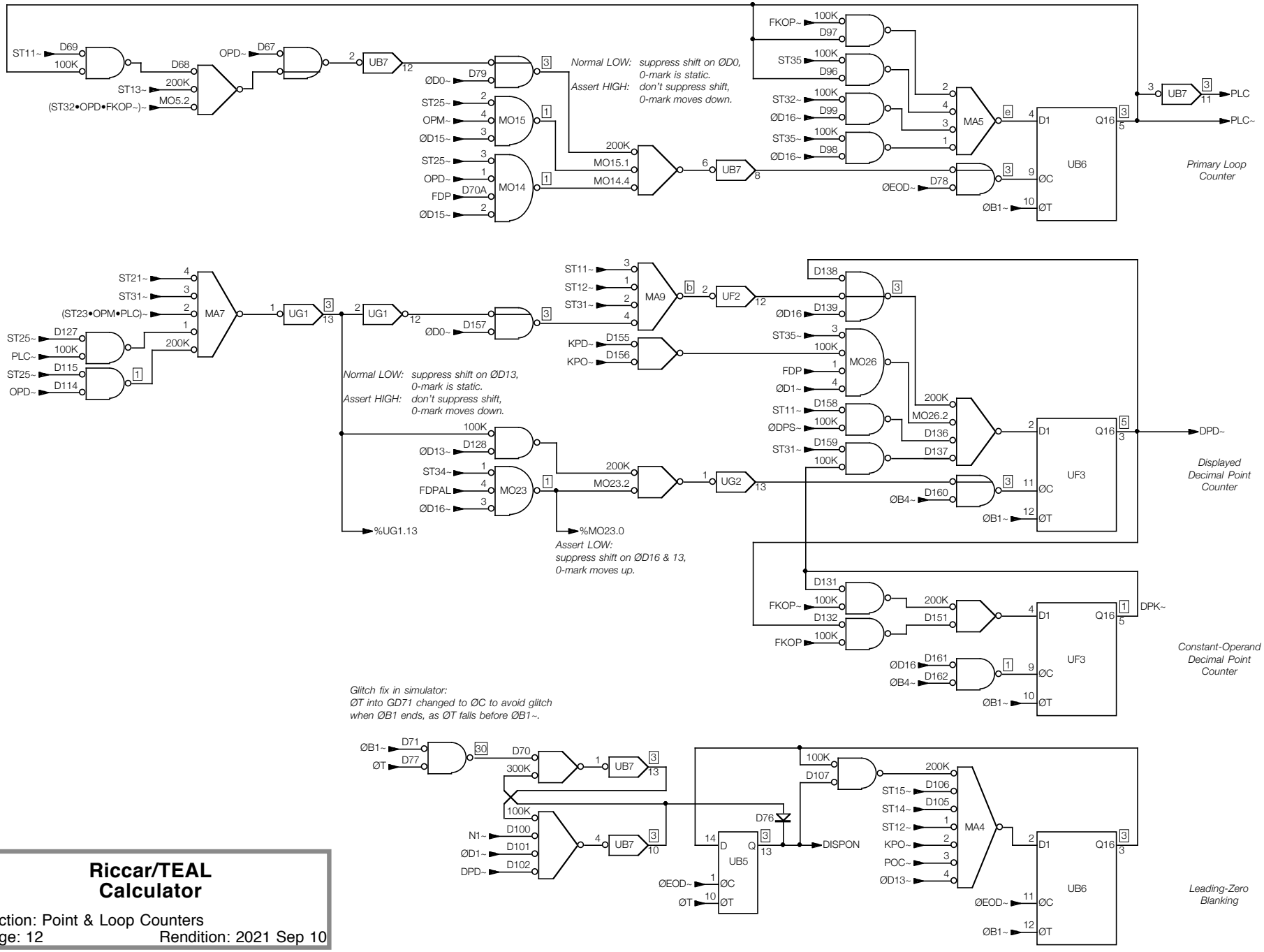

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Section: Point & Loop Counters
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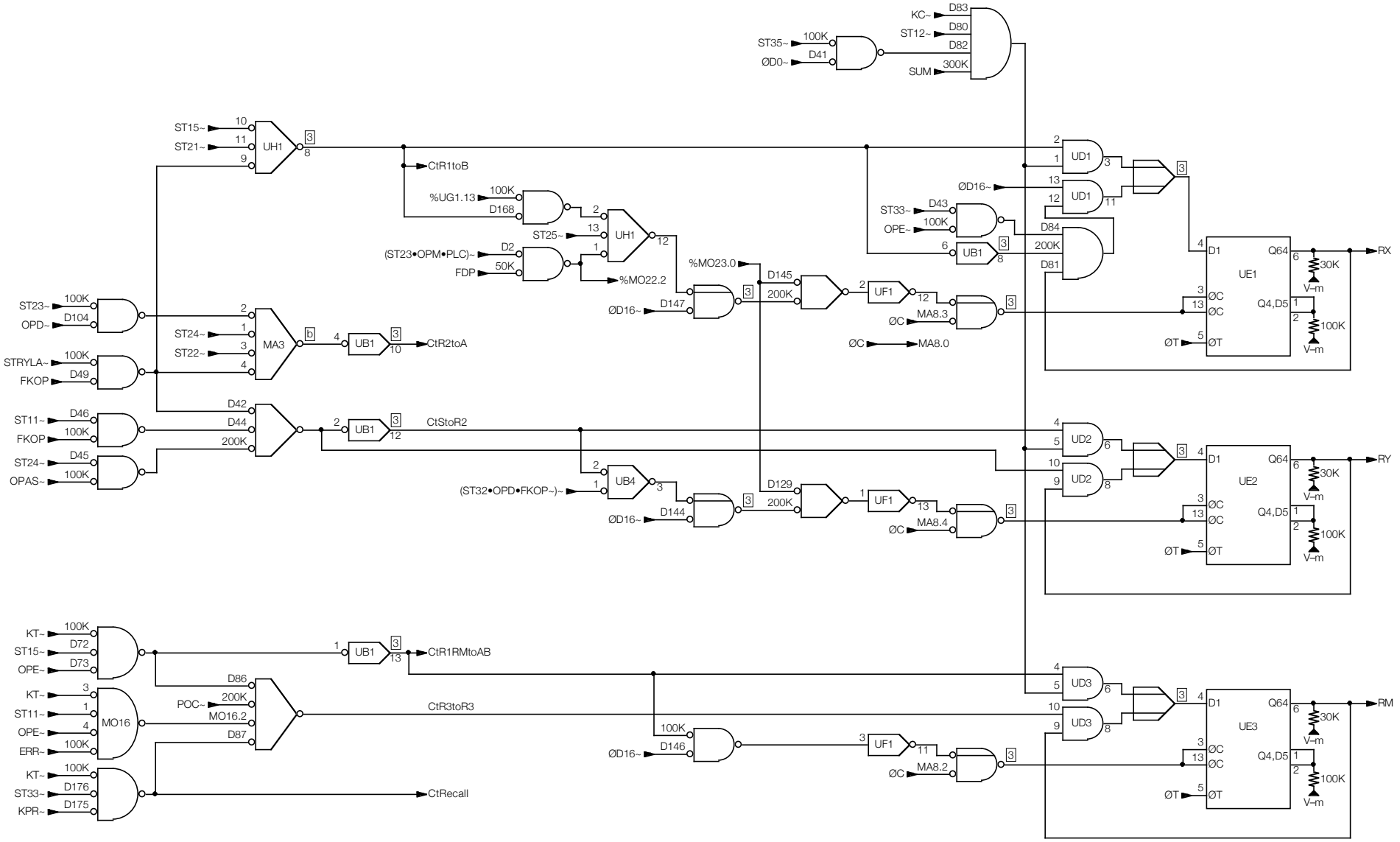

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Section: Registers
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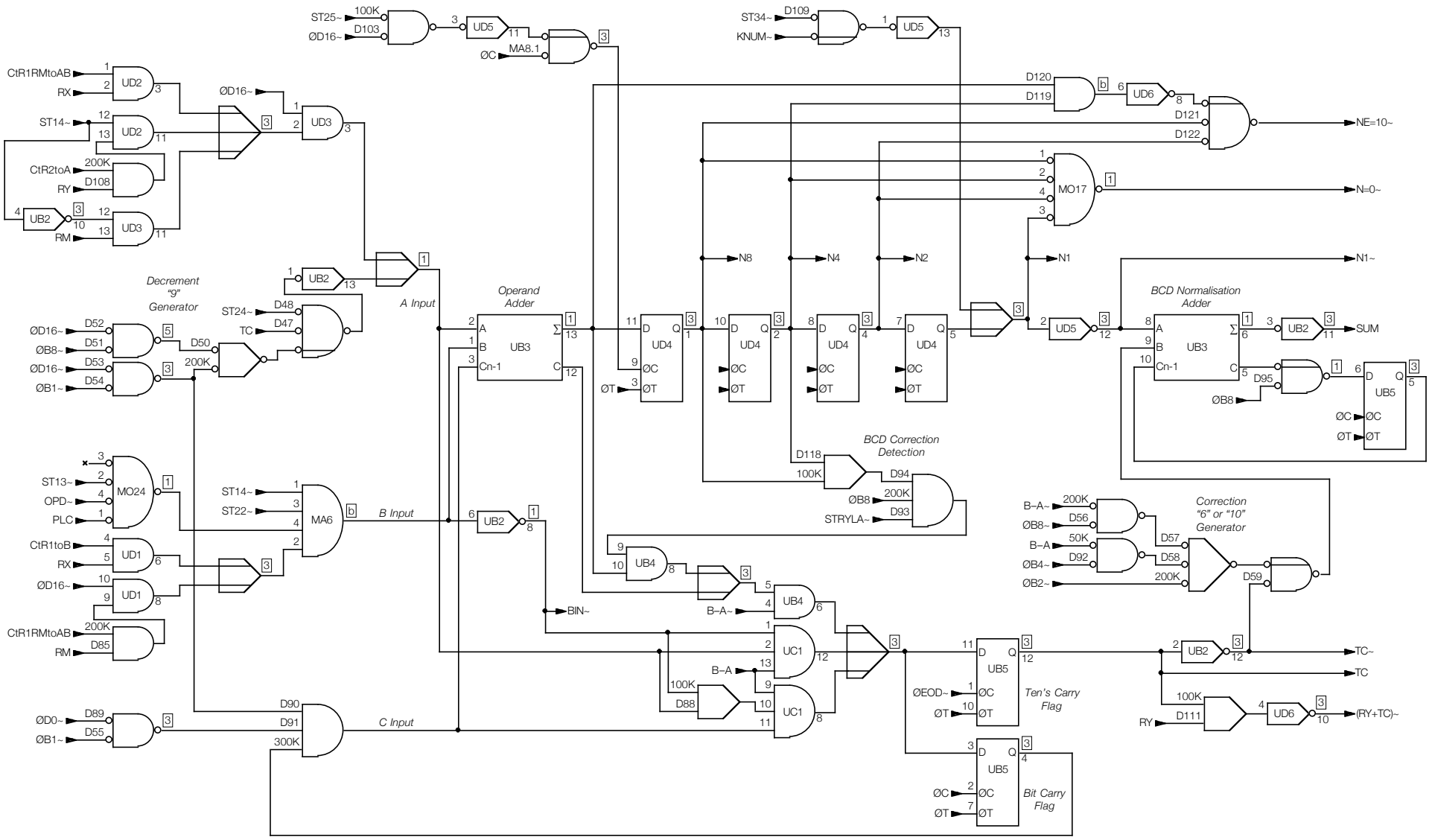

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Section: Arithmetic
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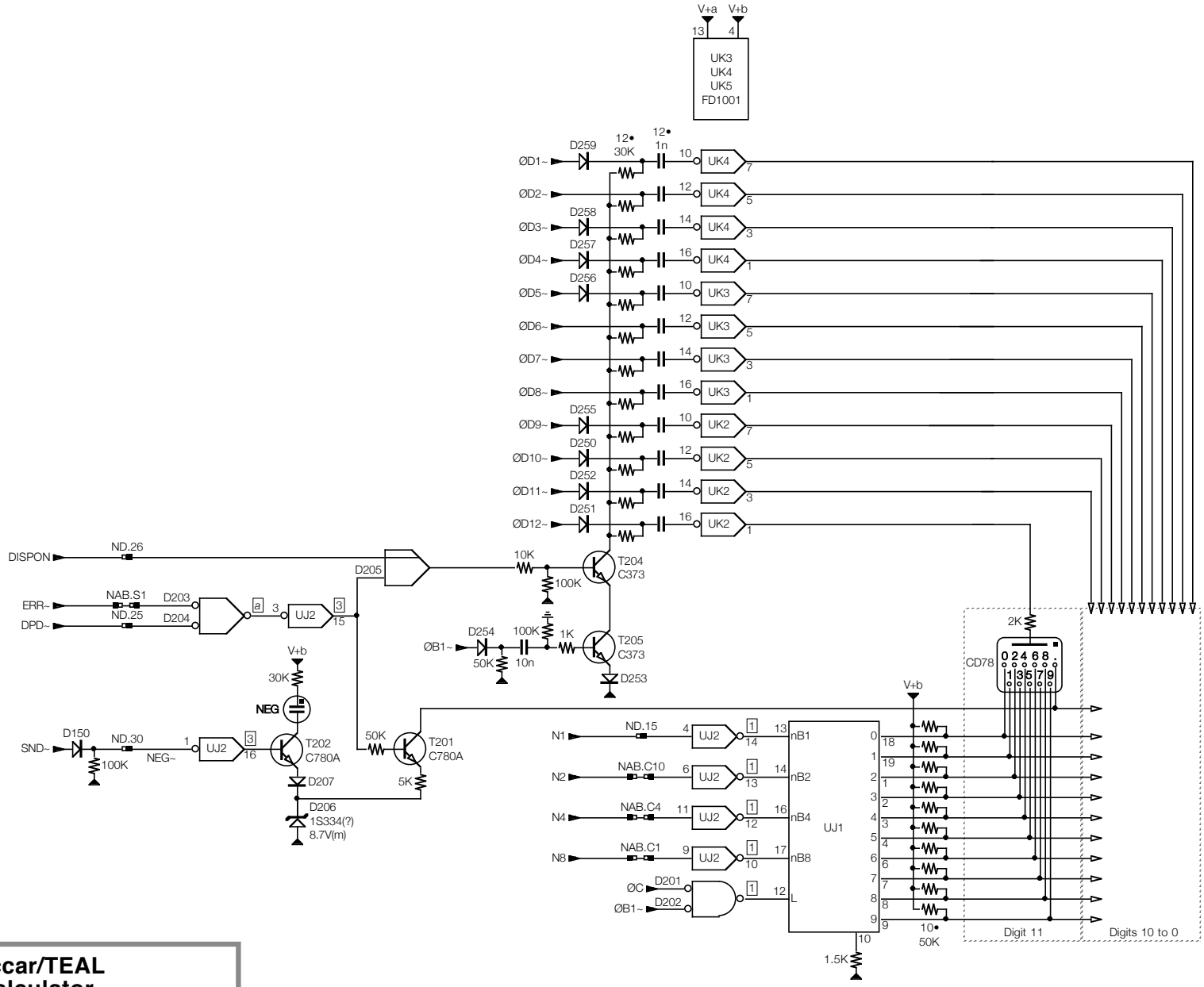

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Section: DIsplay
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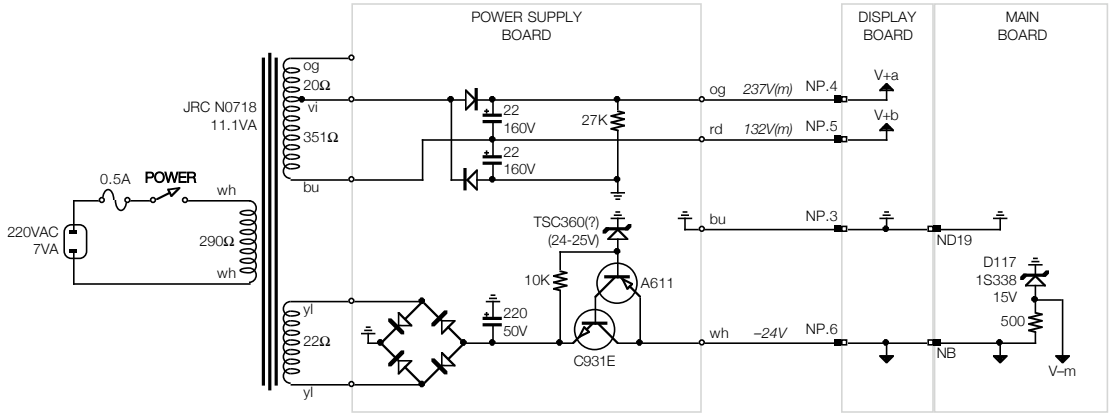

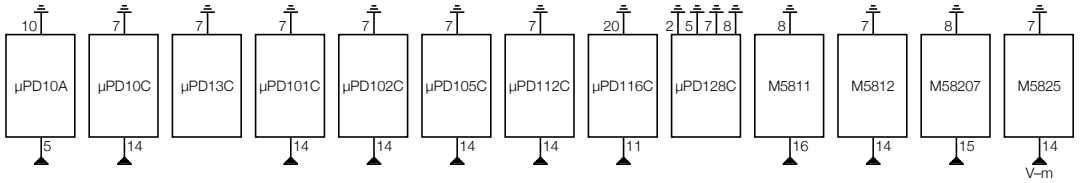

UD4

UK1
UK6

UL2

UB1
UB2
UB7

UD5
UD6

UF1
UF2

UG1
UG2

UH2

UB4

UD1
UD2
UD3

UC1

UH1

UB6

UF3

UB3

UJ1

UJ2
UJ3

UK7

UA1
UA2
UA3

UK5

UL1

UB5

UE1
UE2
UE3

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Section: Power Supply
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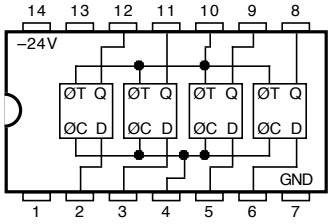
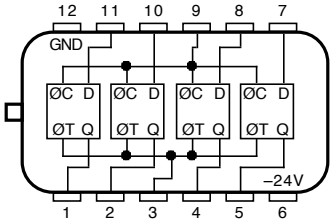
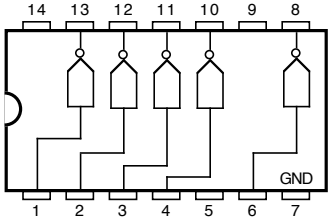
NEC μPD10C



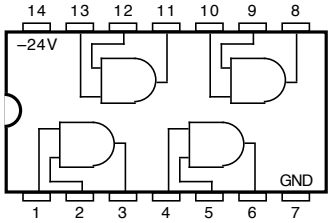
NEC μPD10A



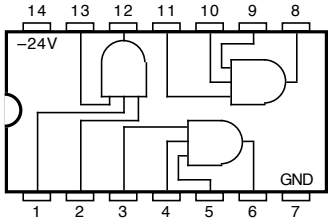
NEC μPD13C



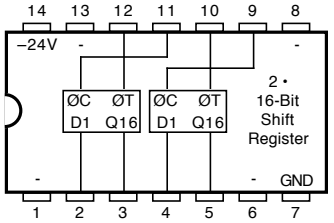
NEC μPD101C



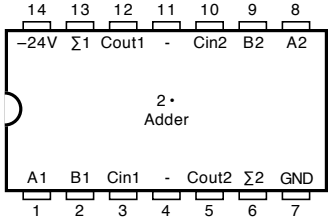
NEC μPD102C



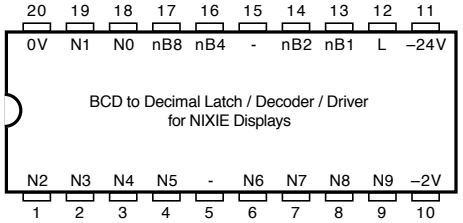
NEC μPD105C



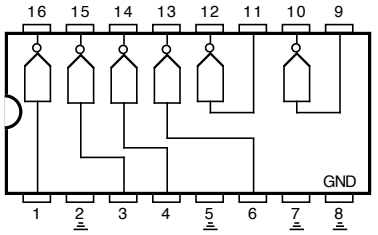
NEC μPD112C



NEC μPD116C

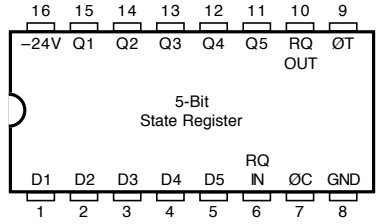


NEC μPD128C

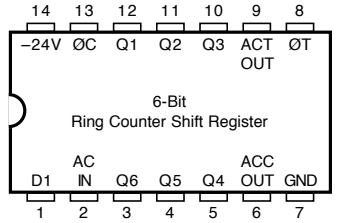


2,5,7,8: GND in 3 instances of use

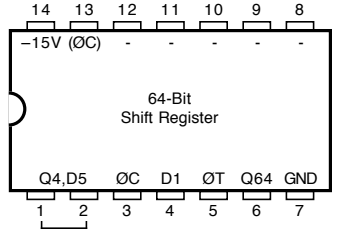
Mitsubishi M5811



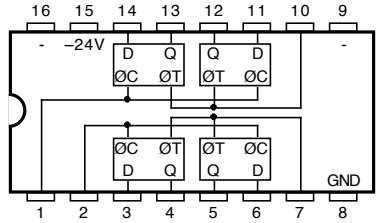
Mitsubishi M5812



Mitsubishi M5825

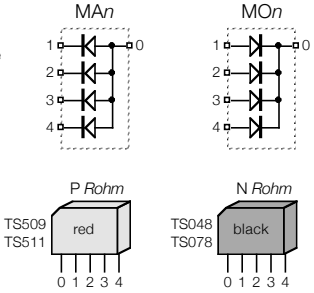


Mitsubishi M58207



Rohm diode modules are distinguished by the case color and N or P embossed on the top.

Silver labeling on the side does not appear to be a part/type number.



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Section: IC & Module Pinouts
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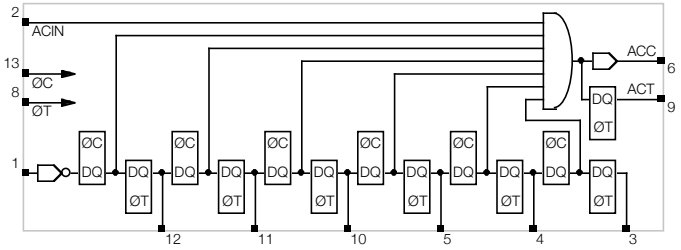
M5812
6-Bit Ring Counter Shift Register

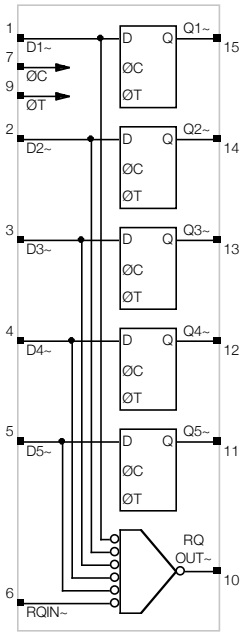
Outputs are active-low.
Flip-flops are gated-active-low.
AC: All Clear. These pins are used to form a ring counter with one or more of these ICs.



M5811
5-Bit State Register

States are active-low.

RQ: State request. With external clock-inhibition circuitry controlled by RQOUT, if no D inputs are requesting a state, the current state will loop. The loop exits when a D input goes low.

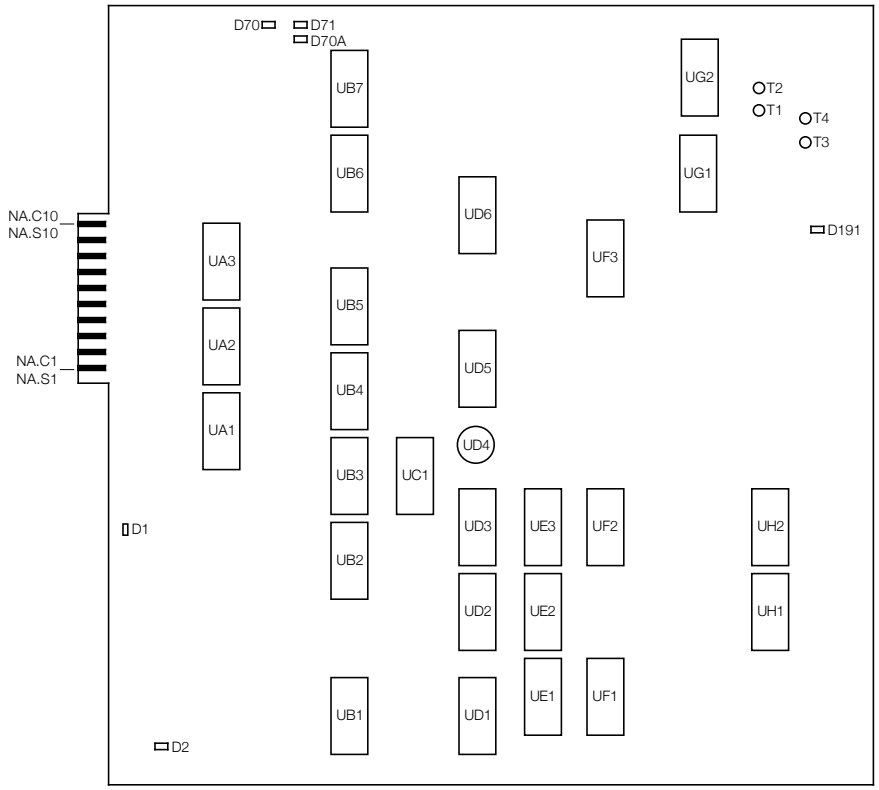


• These diagrams present a functional-equivalent internal structure for the ICs, as inferred from reasoning and observation of behavior.

Signal Names

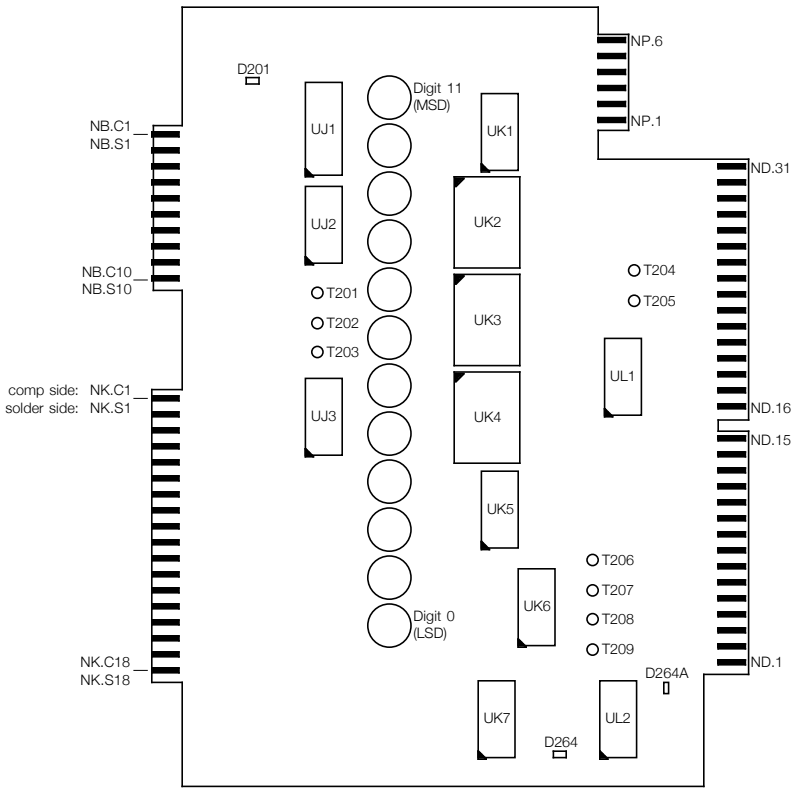
Section	Signal	Description
Timing	ØC	Master clock, data capture phase.
	ØT	Master clock, transition outputs phase.
	ØB1,2,4,8	Bit periods to distinguish the 4 bits of a digit.
	ØD0::16	Digit periods to distinguish the digits of a number.
	ØEOD	Capture pulse at the end of a digit.
	ØEON	Capture pulse at the end of number cycle.
	ØDPS	A digit phase as selected by the DP switch.
Keyboard	KNUM	0::9 numeral key bit stream.
	KP…	State-synchronised latches for keypress processing.
	KPN	Process a numeral key.
	KPD	Process the decimal point key.
	KPR	Process the recall key.
	KPO	Process an operation key.
	KC, KCE	Clear keys.
	KT, KK	Tally & constant switches.
Control	STn	Primary states of the control state machine.
	NSTn	Next state for the state machine.
	STSUP	Signal to suppress duplicate states in a few instances.
	OPAS	Add/Subtract operation to be performed.
	OPMD	Multiply/divide operation to be performed.
	OPAM	Add/Multiply.
	OPSD	Subract/Divide.
	OPM	Multiply operation.
	OPD	Divide operation.
	OPE	Equals operation.
	OPEA, OPES	Distinguish equal-add from equal-subtract operations.
	FKOP	Flag indicating a constant-operand has been entered.
	ERR	Latched error or overflow state.
	FDAT	Flag catching conditions within the number cycle.
Sign Flags	SND	Sign of the displayed operand.
	SNO	Sign of the other operand.
	SNM	Sign of the tally memory register.
Counters	PLC	Primary loop counter for multiply & divide.
	DPD	Displayed decimal point counter.
	DPK	Constant-operand decimal point counter.
	FDP	Flag indicating the DP has been set in number.
	FDPAL	Flag indicating number has been aligned to the DP switch setting.
Registers	RX	X register bitstream.
	RY	Y register bitstream.
	RM	Tally memory register bitstream.
Arithmetic	A	A input to Arithmetic Unit.
	B	B input to AU.
	B–A	Perform B–A rather than B+A.
	SUM	Output bitstream of sum from AU.
	N1,2,4,8	A digit passing through the AU, BCD bits for numeral to be displayed.
	N=0	The 4 bits of N are zero.
	NE=10	Early indication N is 10: in the next bit period N will equal 10.
	TC	Ten's carry from add/subtract on digit.

- A "~" in a signal name indicates the logical NOT operation.
- The character "•" in a signal name indicates the logical AND operation.
- The character "+" in a signal name indicates the logical OR operation.



Main Board
(component side)

Note reverse count order between NA & NB.



Display Board
(component side)

NP

6	V–24
5	V+b
4	V+a
3	GND
2	-
1	-

ND

31	ØD13~
30	NEG~
29	ØB4~
28	ØD1~
27	ØD12~
26	DISPON
25	DPD~
24	ØD16d~
23	KPO~
22	ØB8
21	ØDPS~
20	FKOP
19	KPR~
18	-
17	POC~
16	ØB2~
15	N1
14	ØT
13	ØC
12	GND
11	ØD0~
10	KNUM~
9	KC~
8	KEA~
7	OPAM~
6	OPSD~
5	KES~
4	OPMD~
3	KT~
2	OPAS~
1	KK

NAB	S	C	
ERR~	1	1	N8
KCE~	2	2	KPN~
OPE~	3	3	KPD~
-	4	4	N4
-	5	5	-
-	6	6	V–24
ØB8~	7	7	ØEON~
ST11~	8	8	-
ØD15~	9	9	-
ØB1~	10	10	N2

NK	S	C	
-	1	1	-
KA~	2	2	ØDPS~
ØD3~	3	3	GND
-	4	4	KCE~
-	5	5	-
KR~	6	6	KT~
KC~	7	7	KP~
KK	8	8	-
KCOM	9	9	KEA~
KES~	10	10	ØD4~
ØD5~	11	11	-
KS~	12	12	KM~
KD~	13	13	K2~
K6~	14	14	K9~
K5~	15	15	K4~
K8~	16	16	K7~
K3~	17	17	K0~
K1~	18	18	ØD1~

Riccar/TEAL Calculator

Section: Connectors & Board Layout
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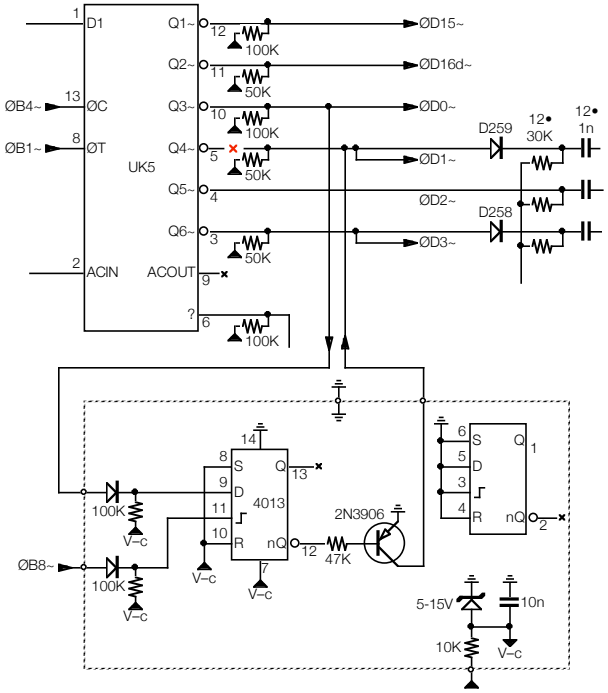
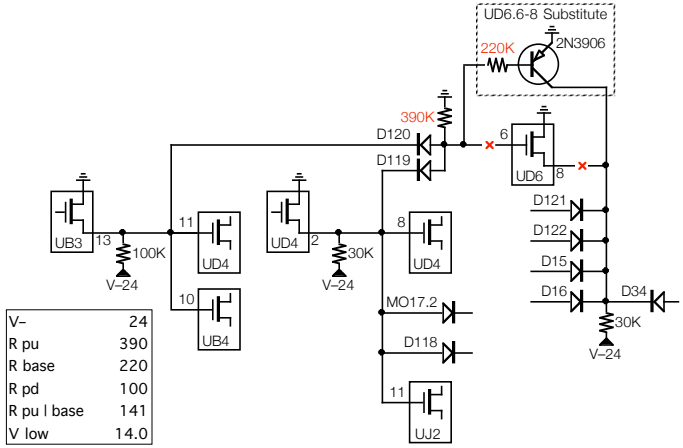


ØD1~ Regeneration

Failed output at UK5.5.

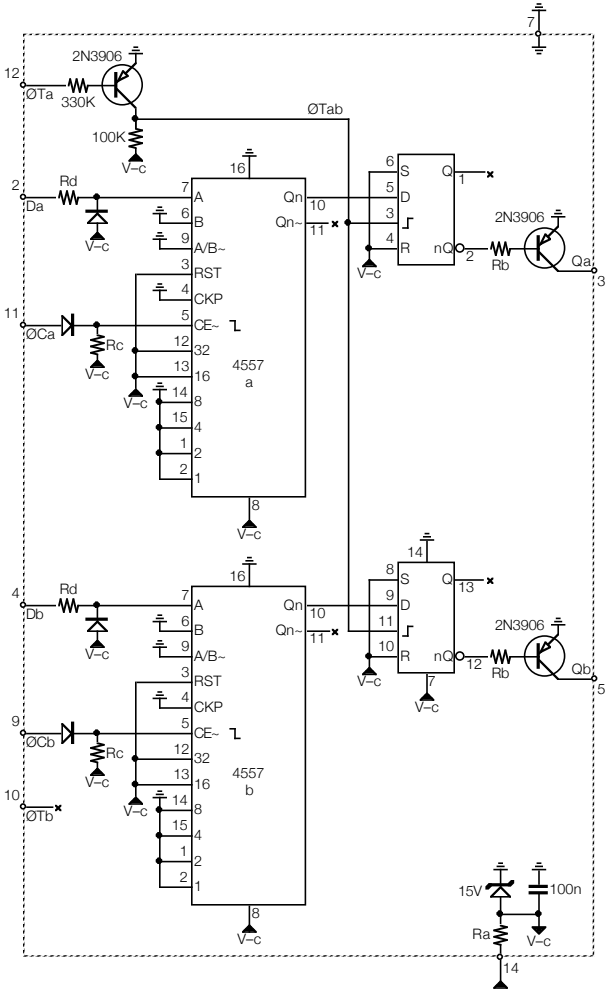
Simple extension of shift register from ØD0~, clocked at end of digit by ØB8~ +edge.

Zener reduces the JMOS supply voltage for the CMOS.
Output transistor provides voltage isolation between CMOS and JMOS.
Diode on inputs similarly provide voltage isolation.

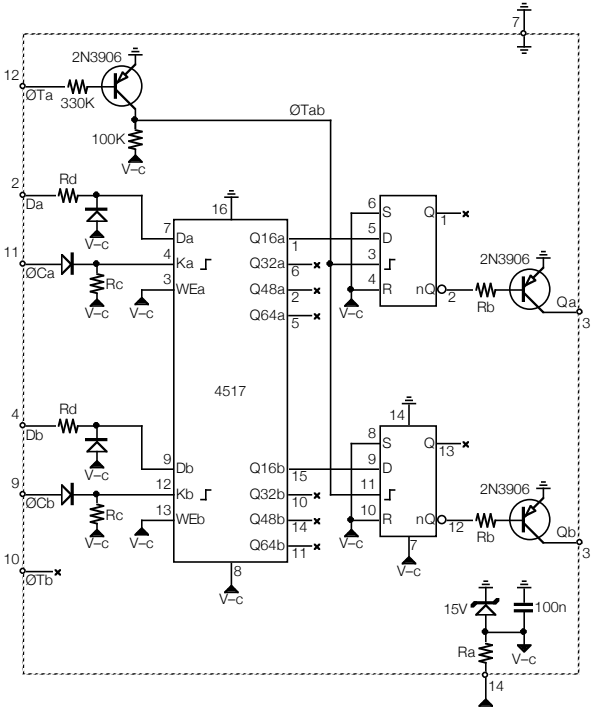


UD6.6-8 Inverter Fix

Replacement for failed MOSFET. Base current for bipolar should be acceptable here.



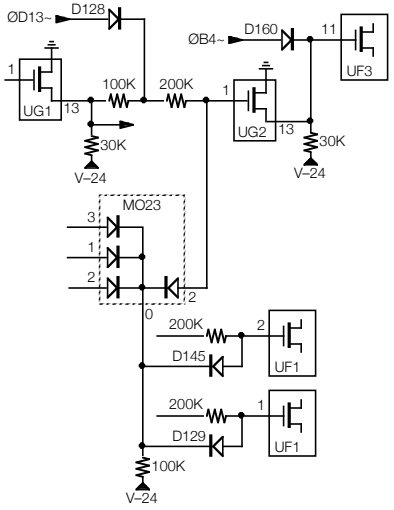
µPD105 Substitute Using Two 4557s



µPD105 Substitute Using 4517

Ra: 3.3K
Rb: 47K / 100K
Rc: 100K :: 470K
Rd: 100K :: 470K

In application for UF3, ØTb is the same as ØTa, thus pin 12 may serve as ØT for both sections a & b.

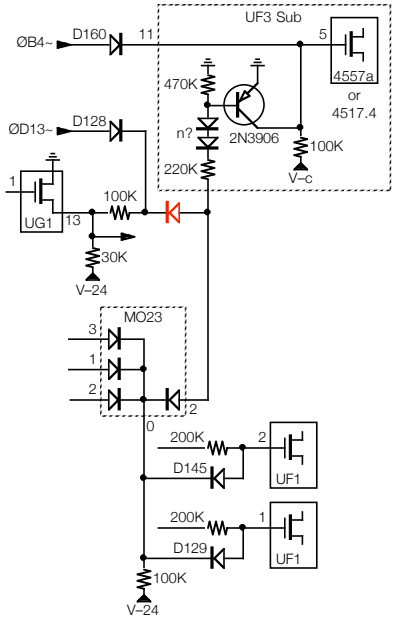


UG2.1,13 Presence in Original Calculator Circuit

VLOWmax+ == maximum positive level for the LOW state of signal.

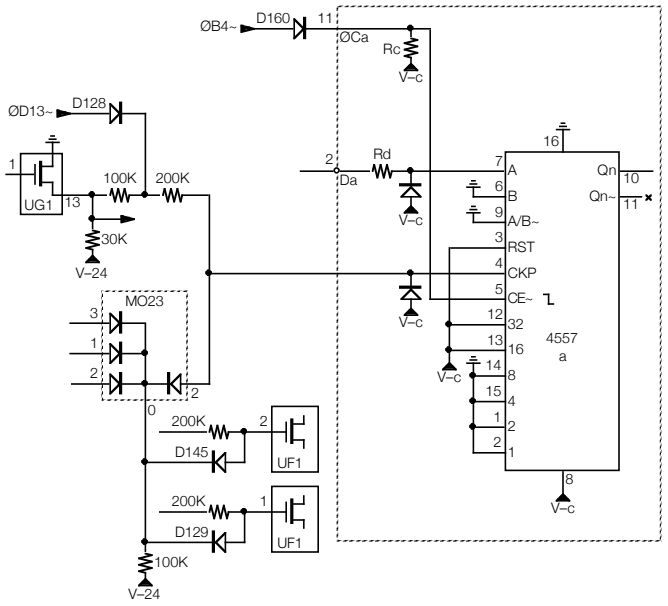
Vlowmax+ can go quite high in this circuit as under some situations all three of the 200K R, effectively in parallel, can be conducting current drawn through the MO23.0 100K R.

VLOWmax+ ~= –24V * (200K/3) / (100+200K/3) ~= –10V



UG2.1,13 Fix Combined with UF3 Substitute - Scheme A

The 200K R from D128 is replaced with a diode for its logic function, while the current which would have gone through it is 'moved' to be used as the base current for the 2N3906.



UG2.1,13 Fix Combined with UF3 Substitute - Scheme B

Adaptation of the 4557 sub design to take advantage of the clock enable input on the 4557 to do the inversion and clock gating. Unfortunately, not applicable if using the the 4517.

JMOS PMOS FET Characteristics Test