TEAL: IME 41
Calculator

Contents

Notes

- The symbol Ncp denotes a physical connector pin, where *c*=connector and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- The symbol ▲ without an additional label denotes VDD (–24V).
- See also the TEAL/Riccar schematic (madrona.ca/e/eec). A state diagram is included in the Riccar schematic.
- See also the TEAL/Royal Digital I Theory of Operation document (madrona.ca/e/eec).
- This drawing is based on observation of board photographs of two units.
  Photographs, tracings of hidden tracks and measurements supplied by Jef Ongena of Belgium.

Log

- 2023 Aug: Initial drawing / bhilpert.

Differences

Two units of the IME-41 have been examined with several differences observed between the two. These differences and the components involved are noted in blue text , the units distinguished as #J and #S.

The IME-41and Riccar model from TEAL are nearly identical in logic design. Most of the differences between the two IME-41 units bring the #S unit closer to consistency with the Riccar.

Logic Presentation

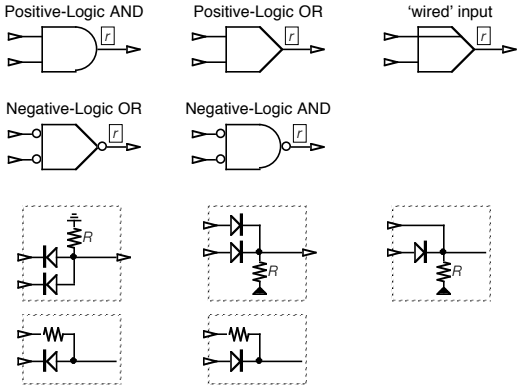
Gate symbols and signal names are presented in accordance with:
logic 1 = GND
logic 0 = V–24

The design uses primarily negative logic in the control portion and positive logic for data and registers.

Logic Implementation

The logic is implemented with a combination of early SSI and MSI MOS integrated circuits from the JMOS family, and discrete DTL. Most gates are constructed from discrete diodes and resistors. Inverters, active gates, flip-flops and more complex logic elements are contained in the integrated circuits. The active elements are open-drain outputs, closing to GND (logic 1), requiring external pull-down resistors to –24V (logic 0).

The internal construction of discrete gates is shown in the following diagrams. A wire–OR or wire–AND construction is indicated by the input line traversing the width of the gate. The design is heavily optimised for component reduction with many gates having one input formed from the pull-up/down load resistor, rather than a diode and fixed-supply resistor.



The diodes may be individual components or contained in 4-diode TSxxx modules. Gate inputs are identified either by a pin number in the case of a diode in a module, the ID of the discrete diode forming the input, or the R value in the case of a resistor.

For gates with fixed-supply load resistors (*R*), to reduce clutter, the resistors are indicated in the schematic by one of the following letters (*r*) in a box by the output.

Symbol (*r*)	Resistance (*R*)	Symbol (*r*)	Resistance (*R*)
#	10K to VDD	a	110K to GND
3	30K to VDD	b	200K to GND
5	50K to VDD		
1	110K to VDD	d	30K to GND
2	200K to VDD	e	300K to GND
30	300K to VDD		

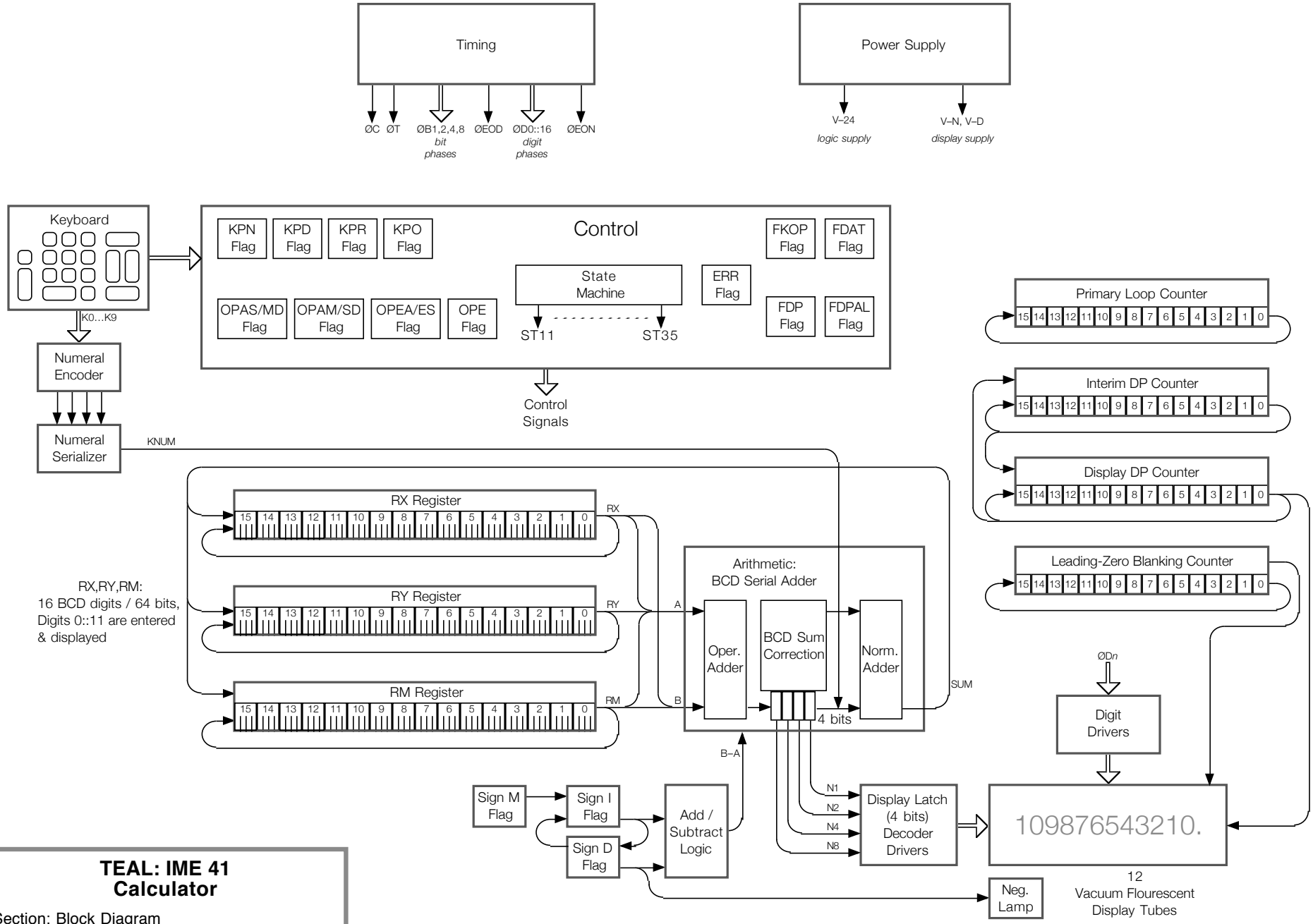
#J: '1' is 110K to VDD.
#S: '1' and 'a' are 100K to VDD . Other 110K are also 100K.

Clocking Scheme

The flip-flops in the JMOS logic family are a form of Master/Slave D-type flip-flop with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while outputs are changed synchronously by a single clock signal.

ØC = Capture Input (master section clock)
ØT = Transition Input (slave section clock)

The state of the D input is captured when ØC is logic 0 (–24V). The Q output is set in accordance with the captured state when ØT goes to logic 0.



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Section: Block Diagram
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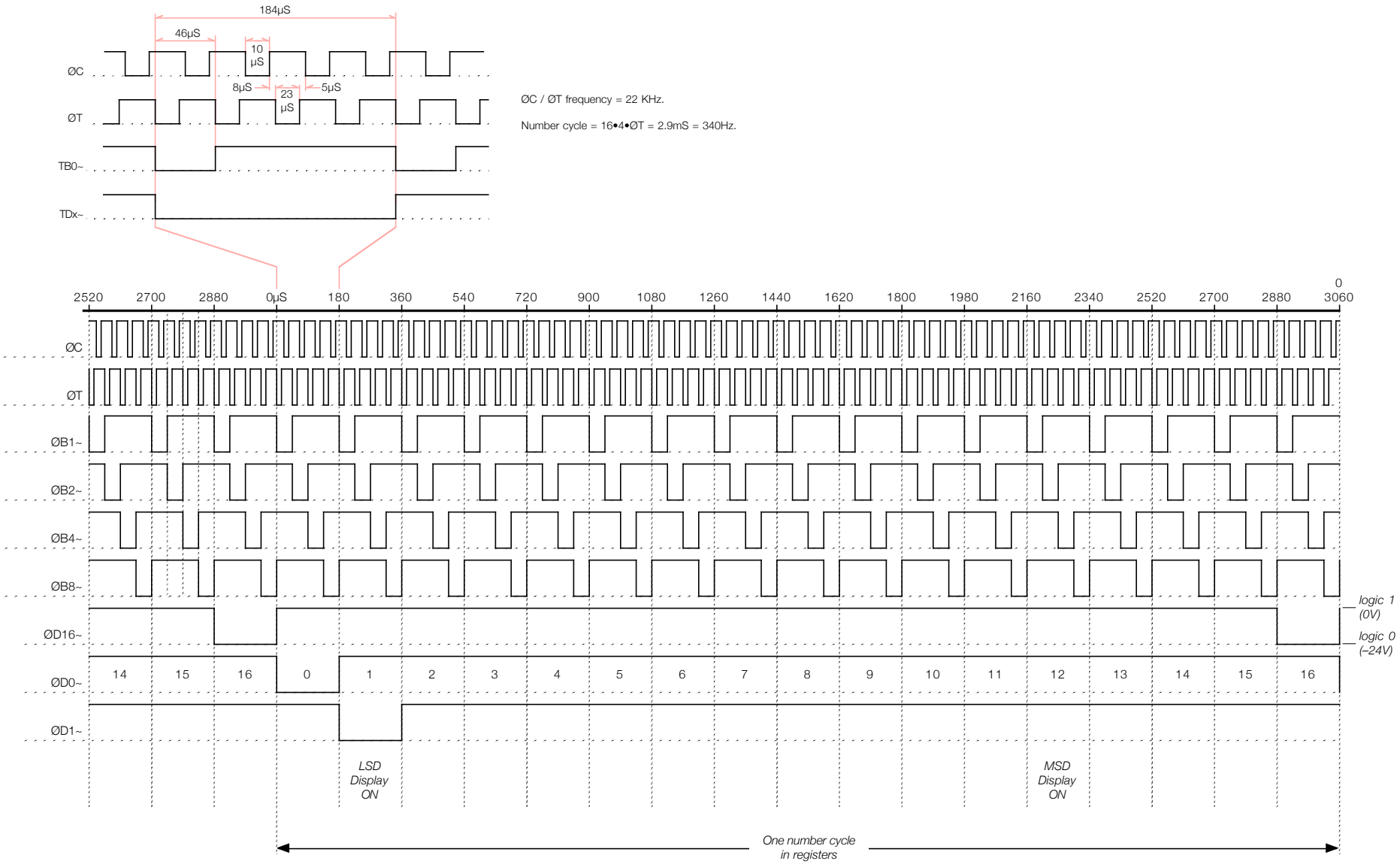

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Section: Timing Diagram
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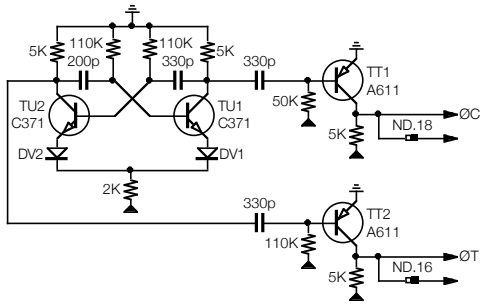
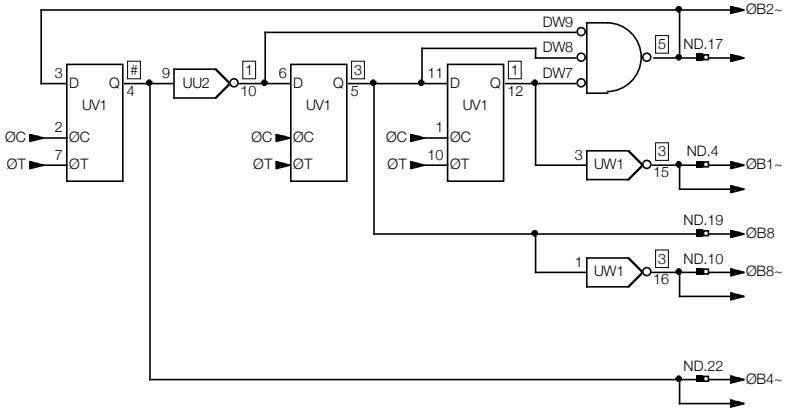
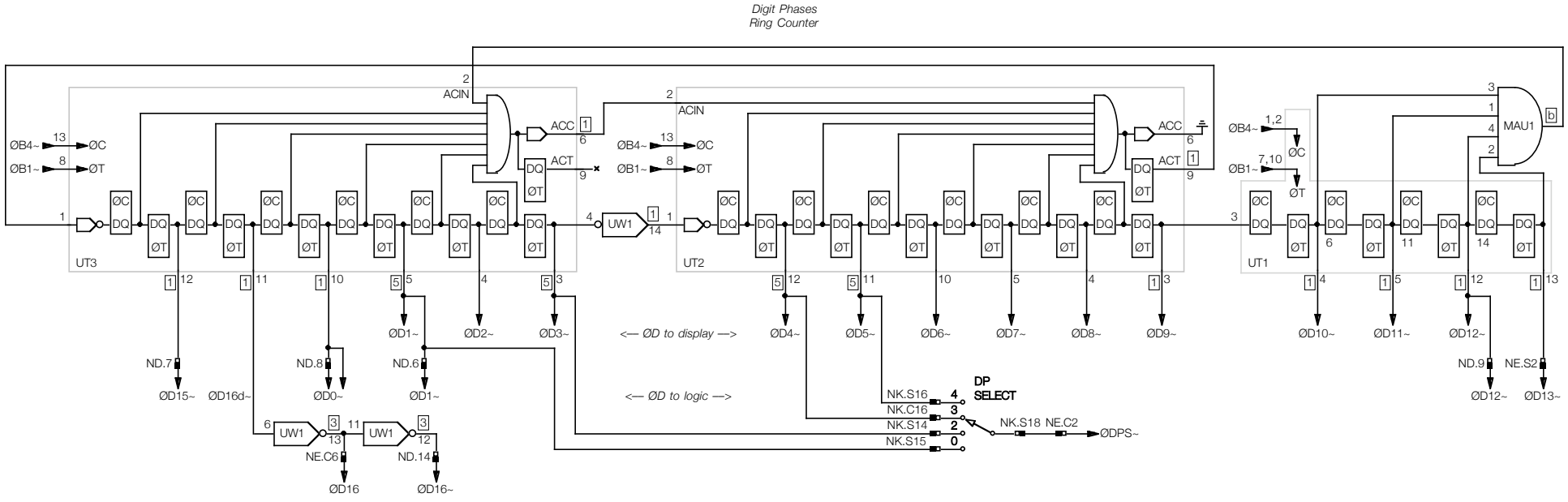
Master Clock

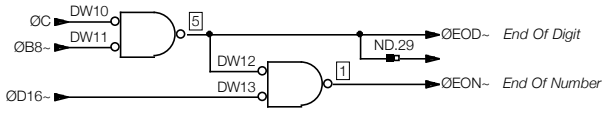


Bit Phases
Ring Counter



Digit Phases
Ring Counter





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Calculator

Section: Timing
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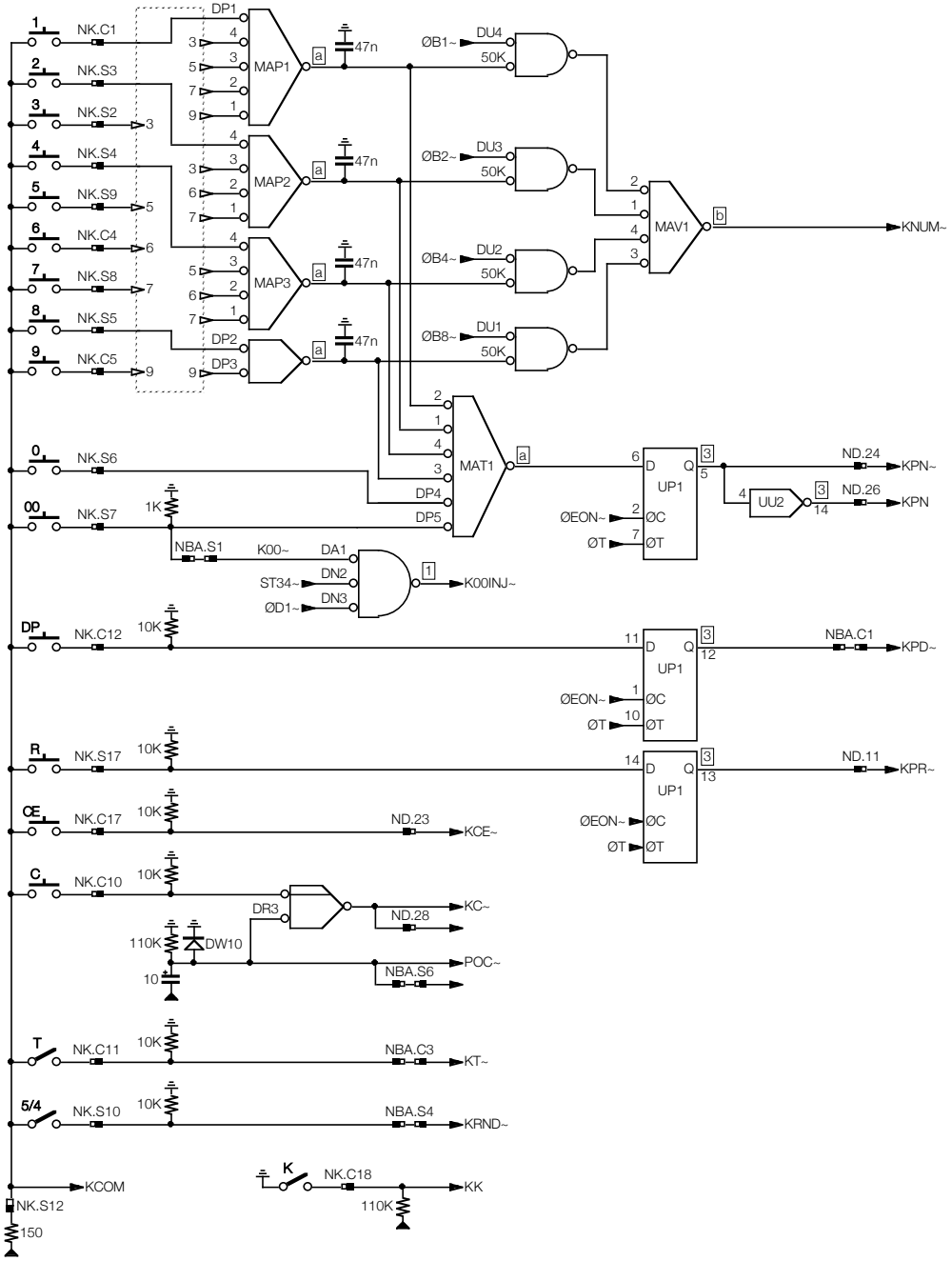

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Section: Keyboard - Numeral Encoding
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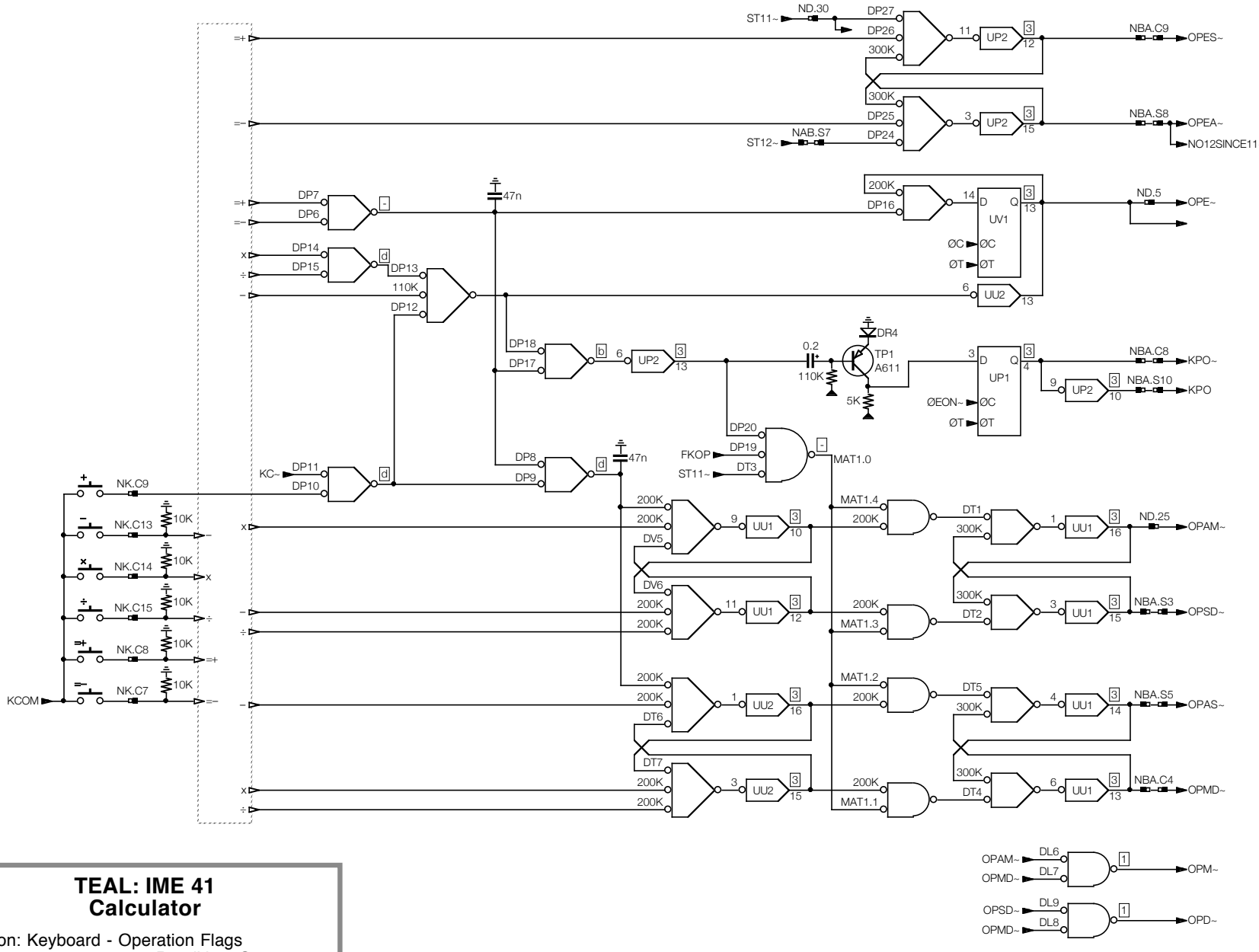

This flag serves for two functions: recording and distinguishing between equals-add and equals-subtract, and indicating whether State 12 has been executed since the most recent execution of State 11.

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Section: Keyboard - Operation Flags
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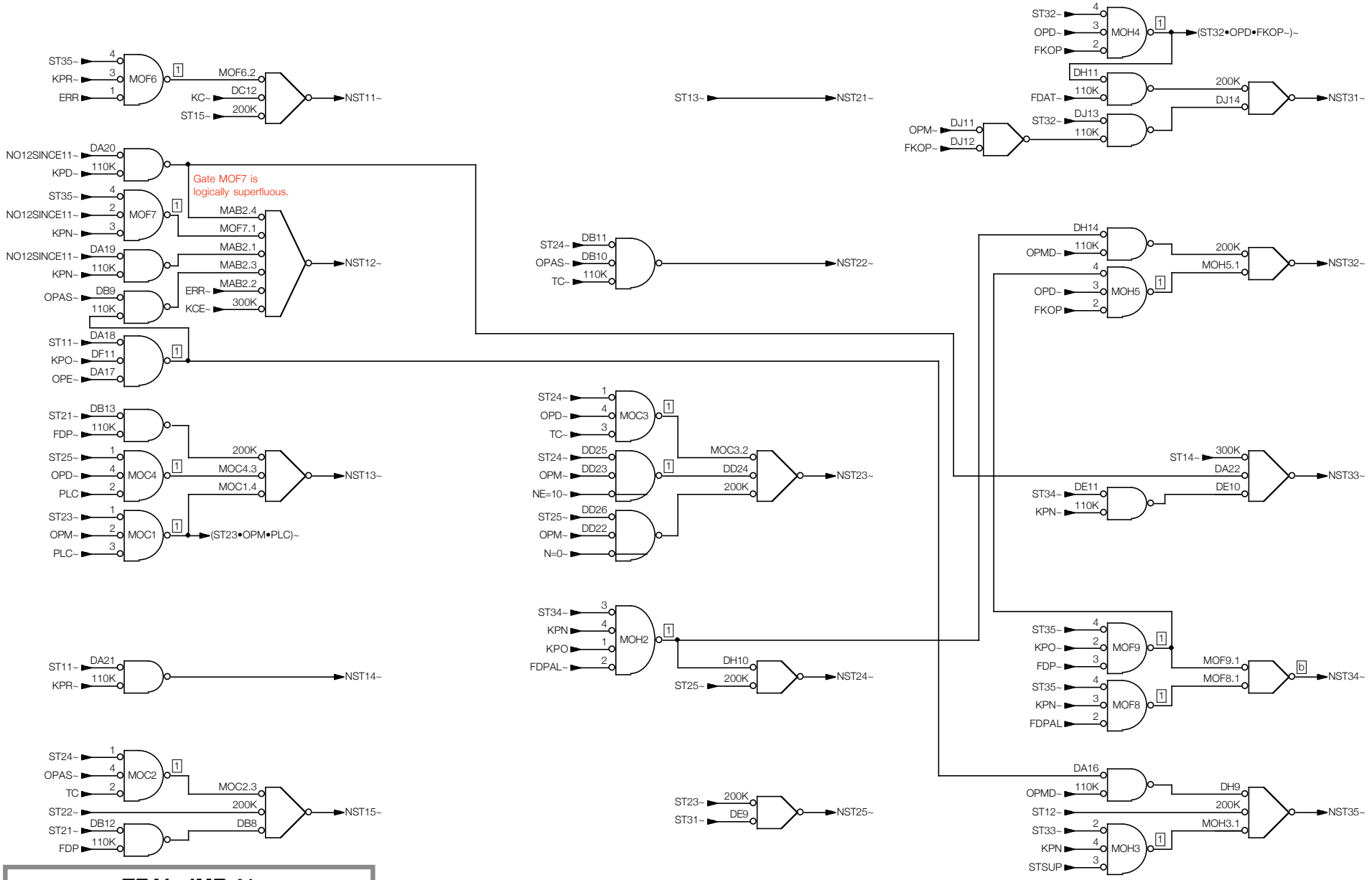

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Section: Control - Next State Logic
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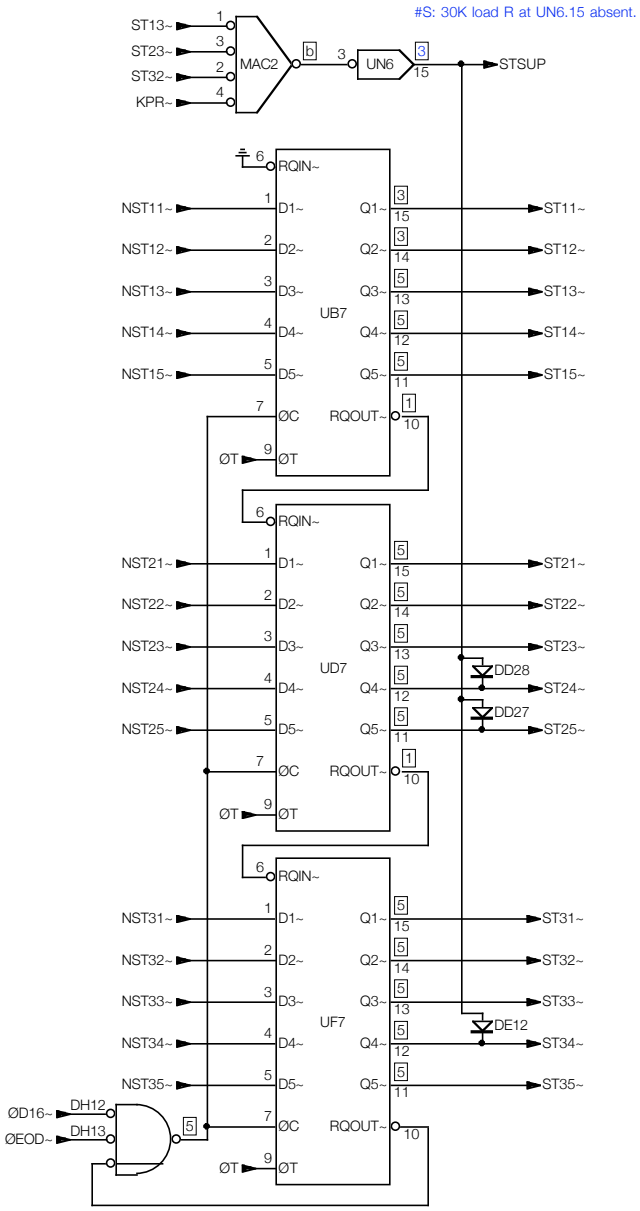
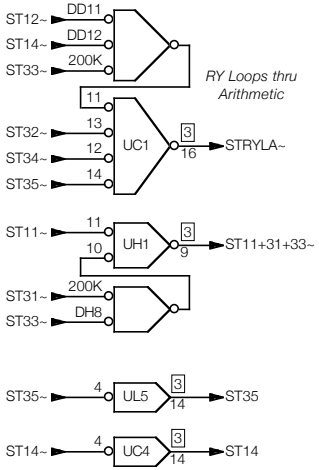
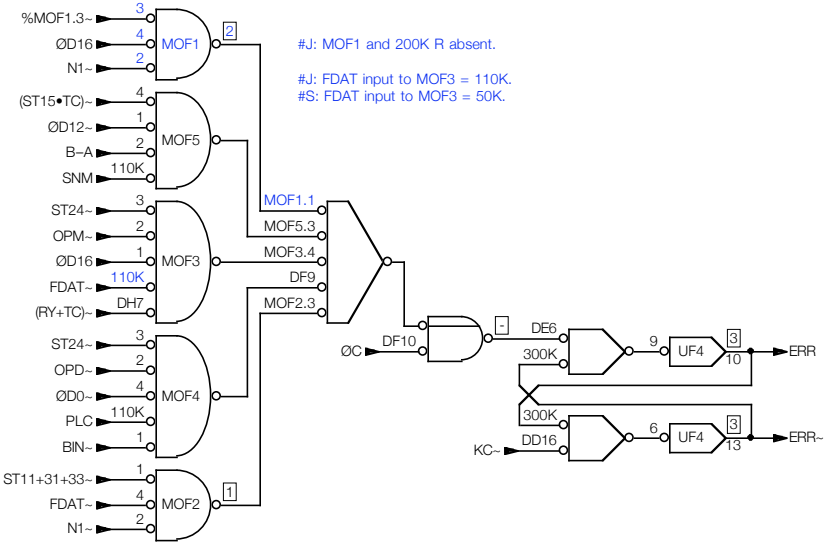


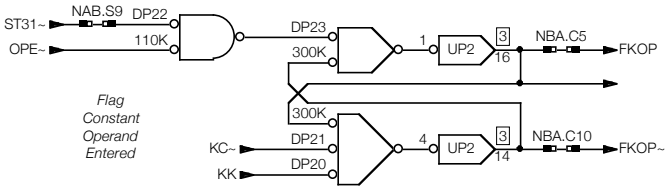
State Suppression:
- ST13 suppresses ST25
- ST13 suppresses ST24
- ST23 suppresses ST24
- ST32 suppresses ST24
- ST32 suppresses ST34

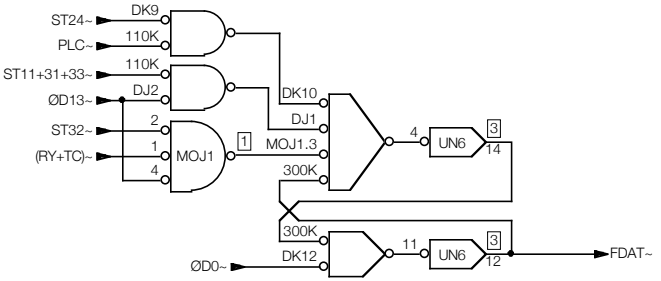
State 12 & 33 are asserted simultaneously during KPD.

State 12 & 35 are asserted simultaneously in error state.









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Section: Control - State Register & Flags
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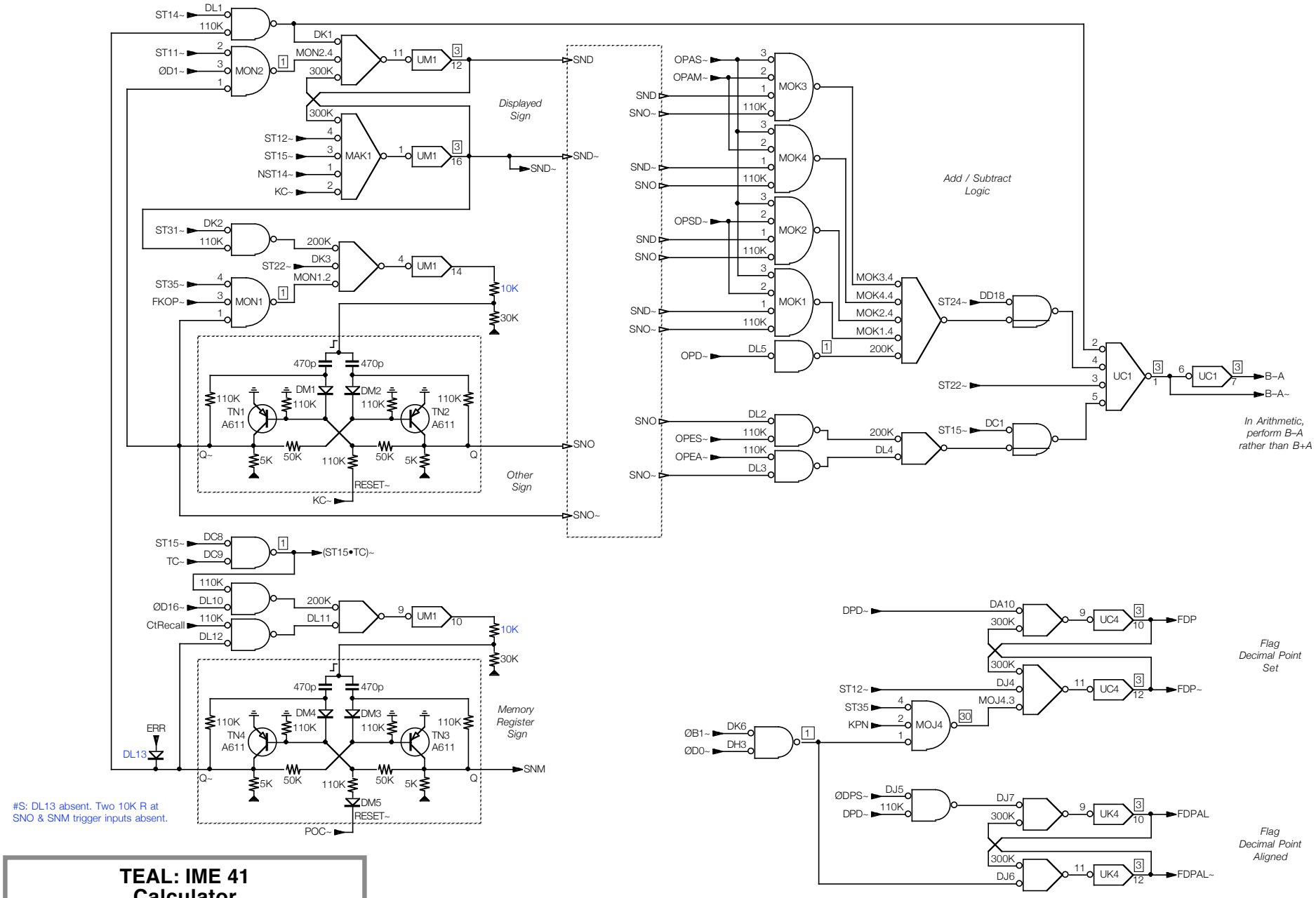

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Section: Sign Flags & A/S Logic, DP Flags
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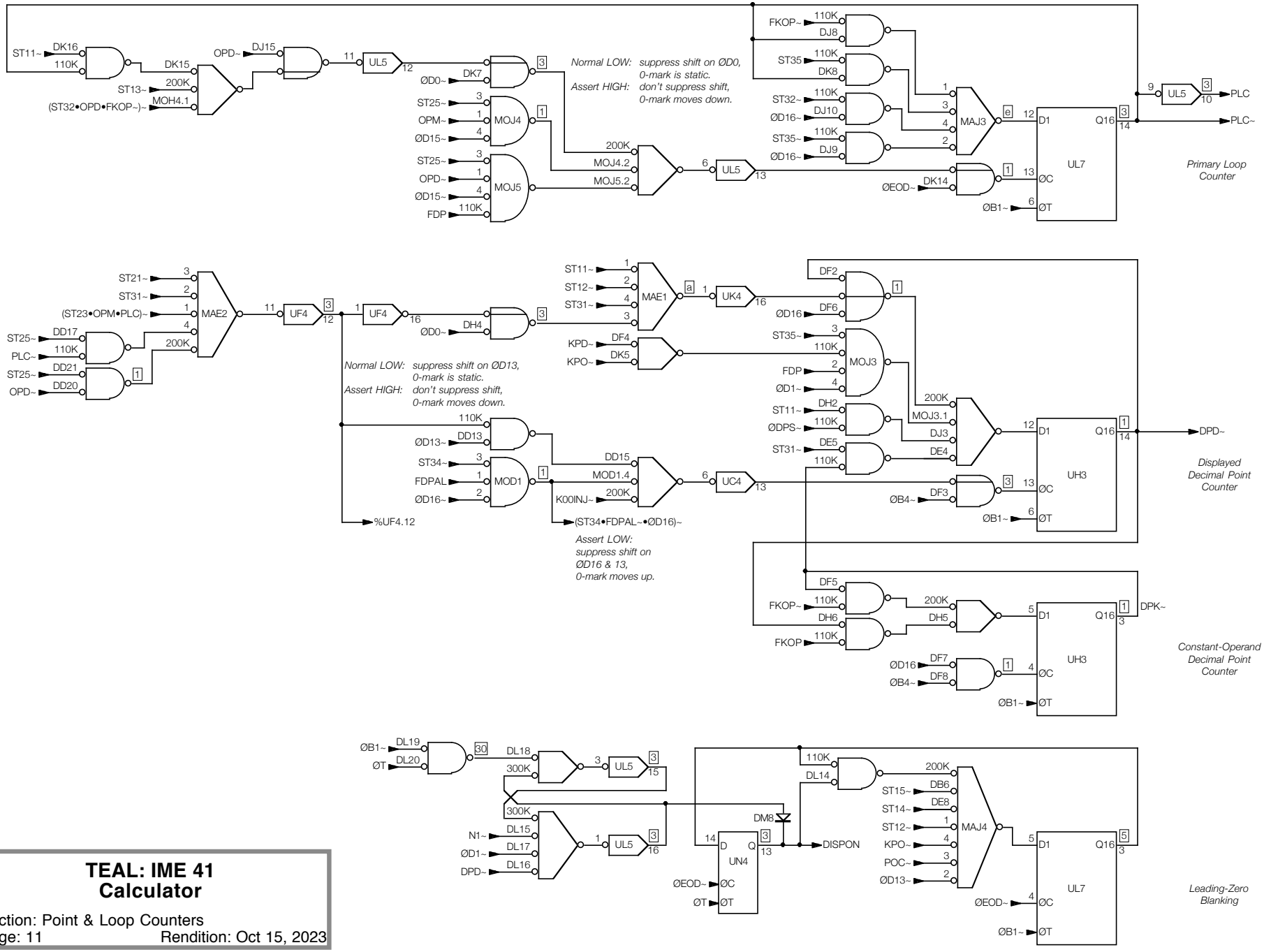

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Section: Point & Loop Counters
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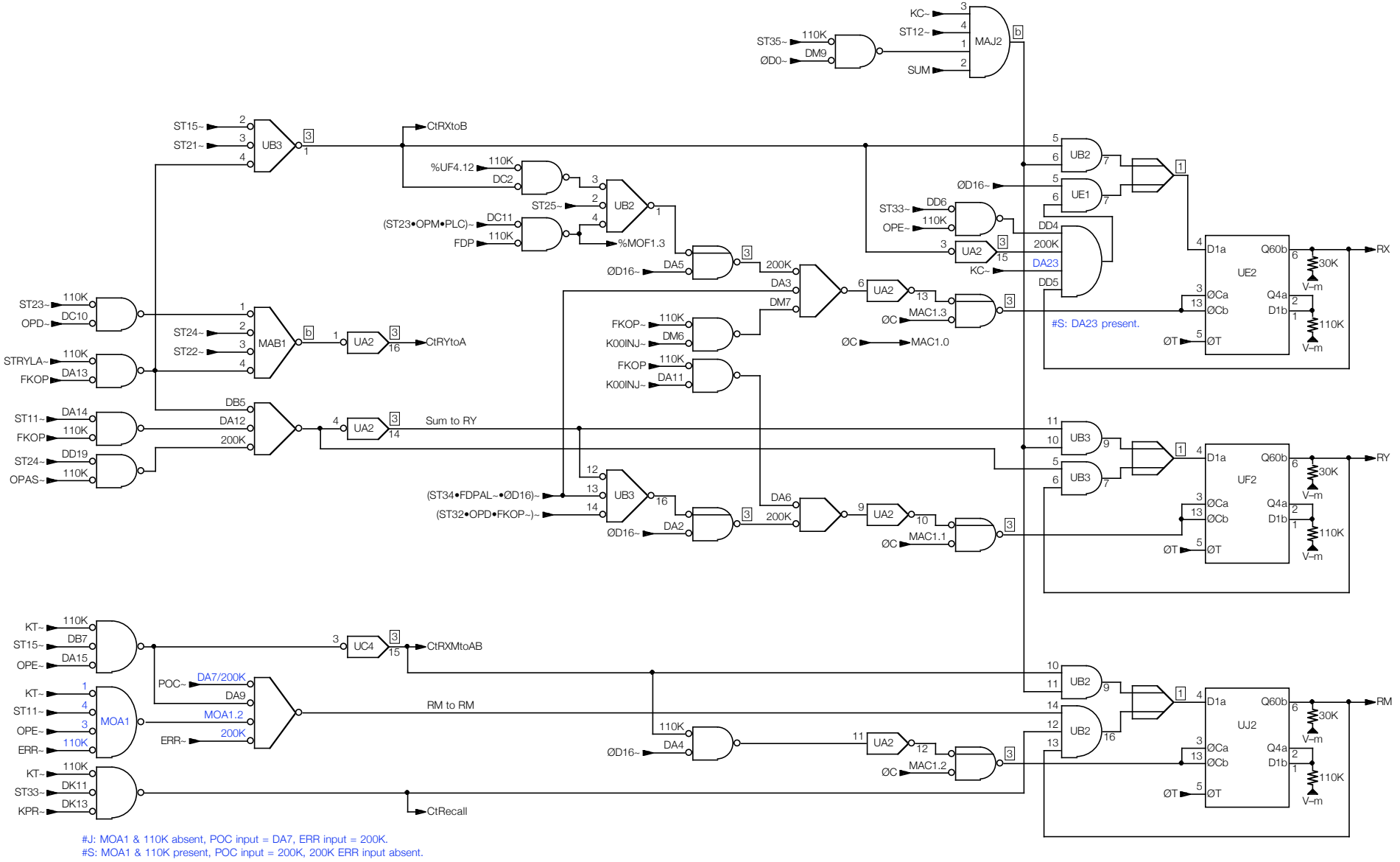

#J: MOA1 & 110K absent, POC input = DA7, ERR input = 200K.
#S: MOA1 & 110K present, POC input = 200K, 200K ERR input absent.

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Section: Registers
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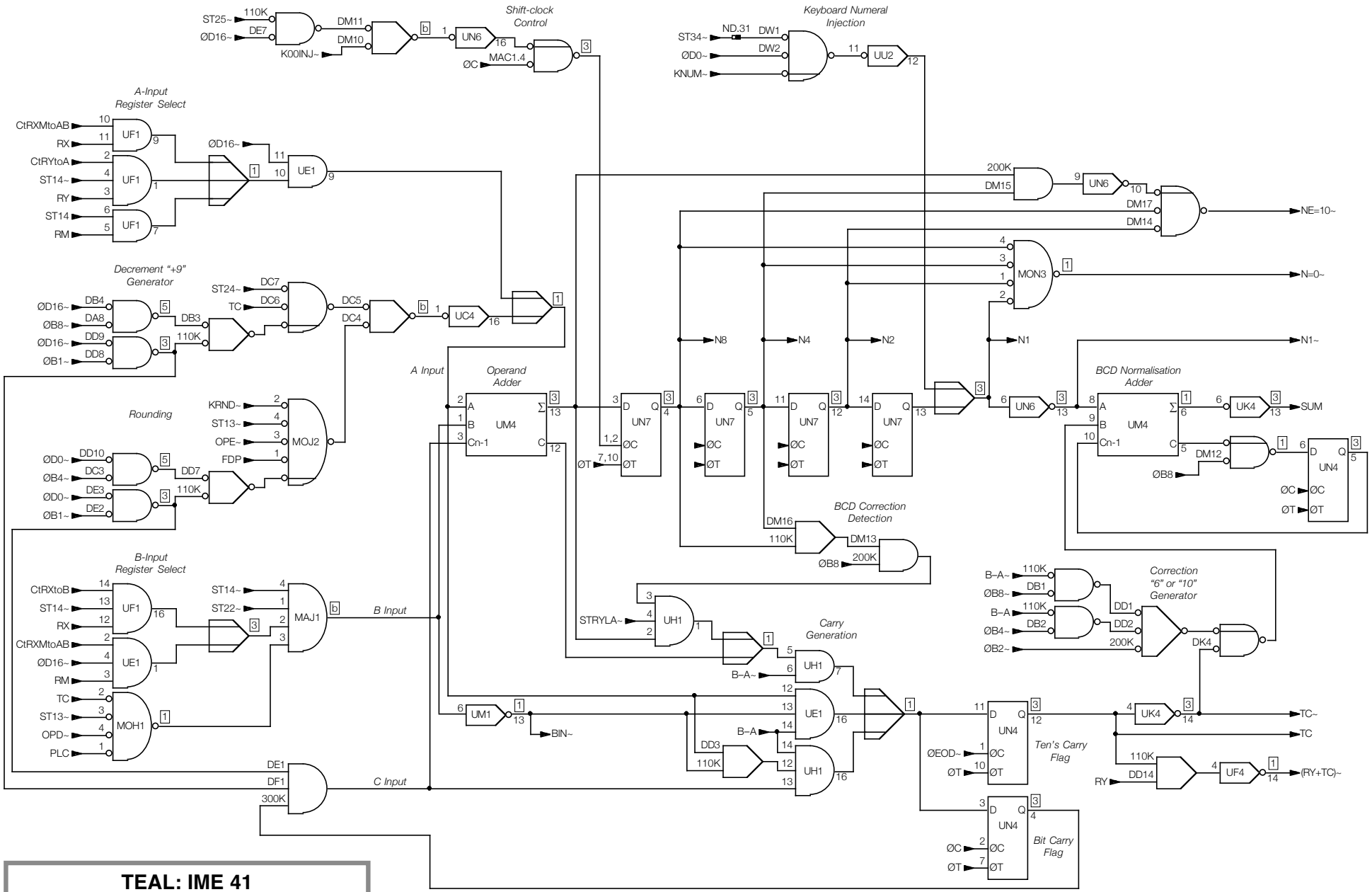

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Section: Arithmetic
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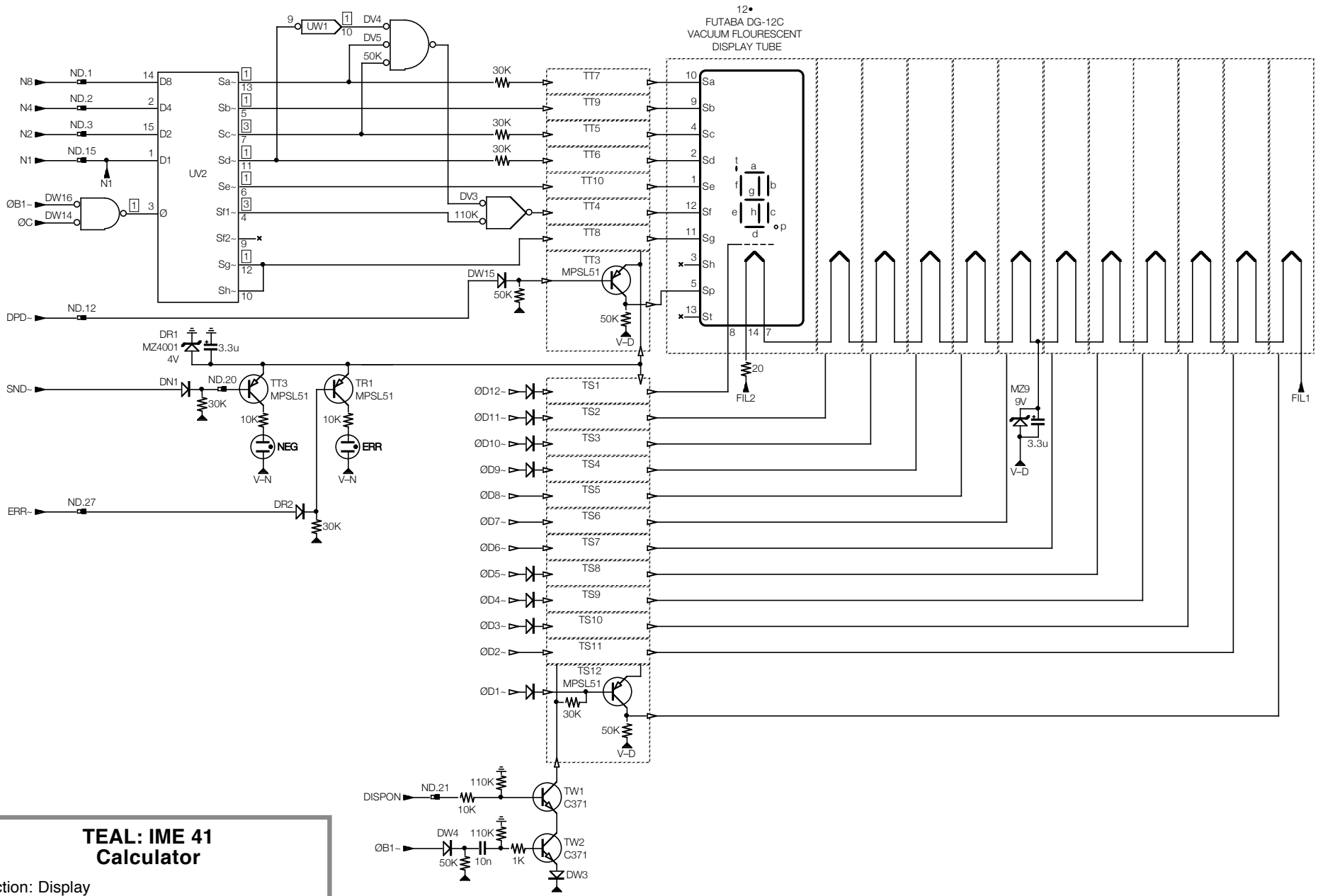

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Section: Display
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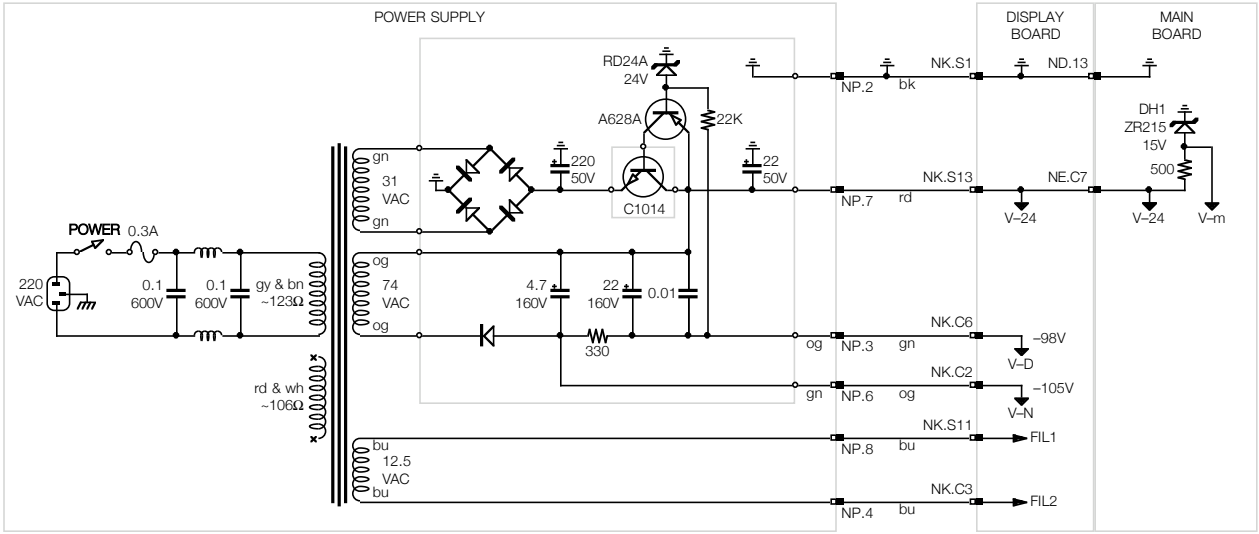
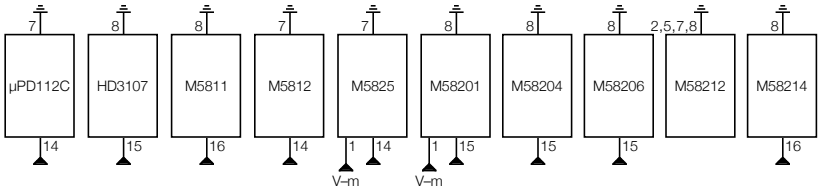




UM4

UN4
UN7

UB7
UD7
UF7

UP1
UT1
UV1

UT2
UT3

UE2
UF2
UJ2

UH3
UL7

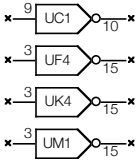
UC1

UE1
UF1
UH1
UB2
UB3

UM1
UA2
UC4
UF4
UK4
UL5
UN6

UP2
UU1
UU2
UW1

UV2



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Section: Power Supply
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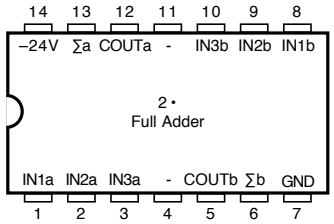
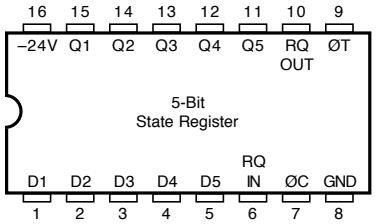
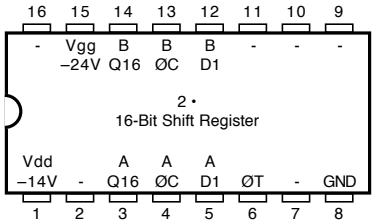
NEC
μPD112C



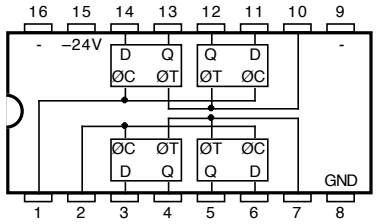
Mitsubishi
M5811



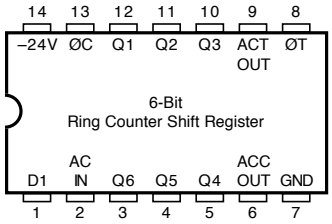
Mitsubishi
M58201



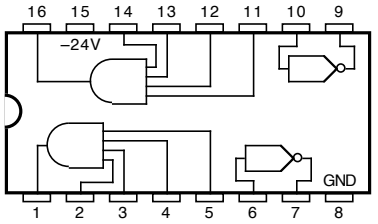
Hitachi
HD3107



Mitsubishi
M5812

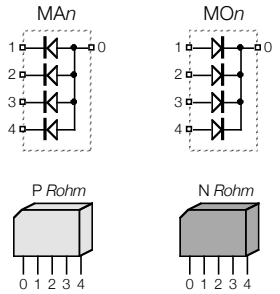


Mitsubishi
M58204



Rohm diode modules are distinguished by N or P embossed on the top.

Silver labeling on the side does not appear to be a part/type number.



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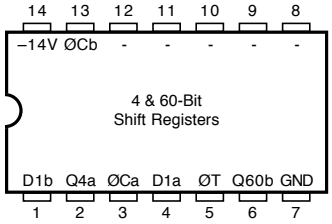
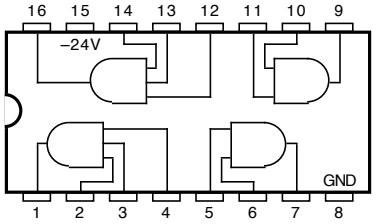
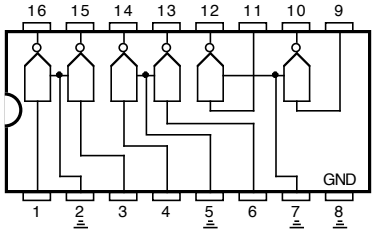
M5825



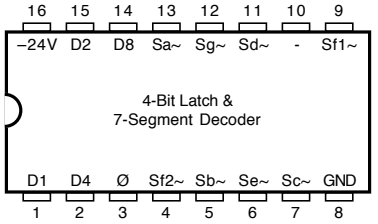
Mitsubishi
M58206



Mitsubishi
M58212



Mitsubishi
M58214



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Section: IC & Module Pinouts
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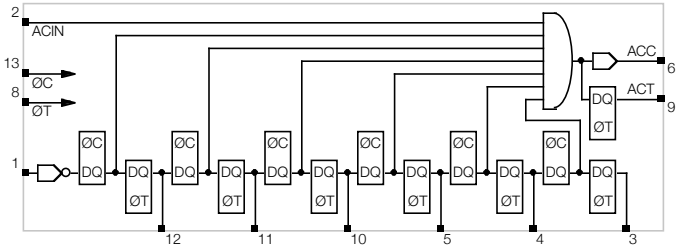
M5812
6-Bit Ring Counter Shift Register

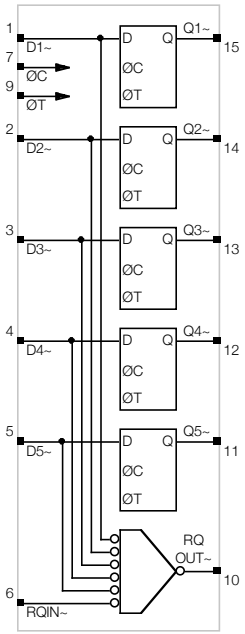
Outputs are active-low.
Flip-flops are gated-active-low.
AC: All Clear. These pins are used to form a ring counter with one or more of these ICs.



M5811
5-Bit State Register

States are active-low.

RQ: State request. With external clock-inhibition circuitry controlled by RQOUT, if no D inputs are requesting a state, the current state will loop. The loop exits when a D input goes low.

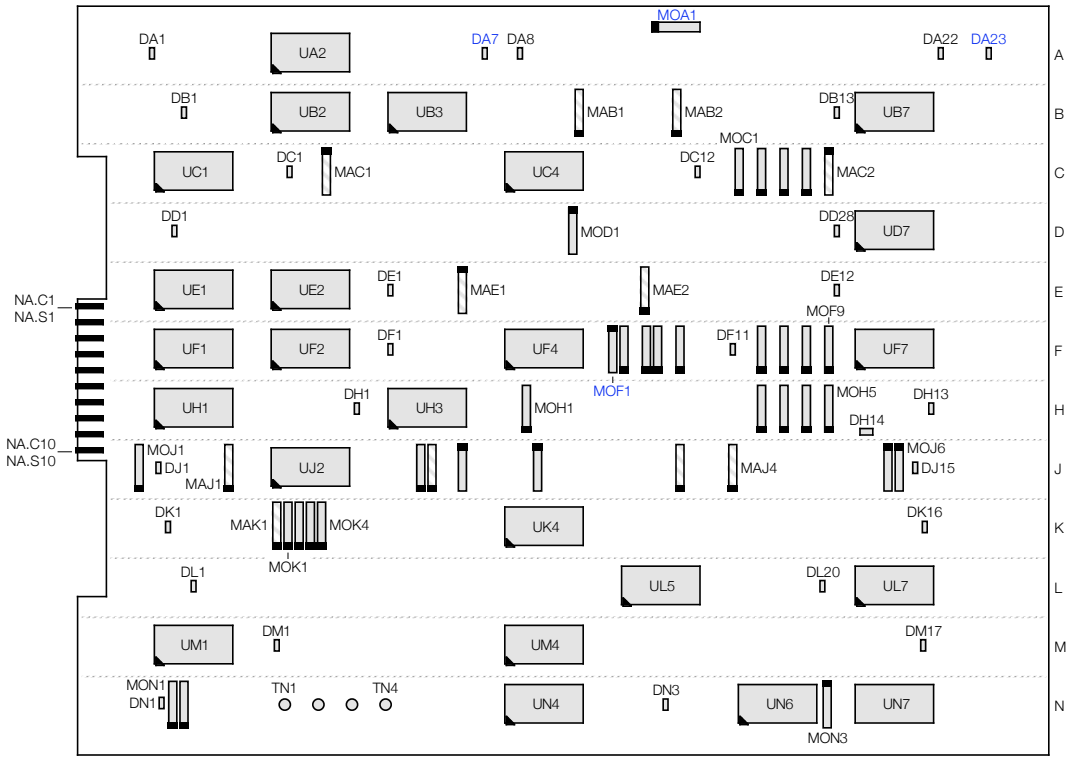


• These diagrams present a functional-equivalent internal structure for the ICs, as inferred from reasoning and observation of behavior.

Signal Names

Section	Signal	Description
Timing	ØC	Master clock, data capture phase.
	ØT	Master clock, transition outputs phase.
	ØB1,2,4,8	Bit periods to distinguish the 4 bits of a digit.
	ØD0::16	Digit periods to distinguish the digits of a number.
	ØEOD	Capture pulse at the end of a digit.
	ØEON	Capture pulse at the end of number cycle.
	ØDPS	A digit phase as selected by the DP switch.
Keyboard	KNUM	0::9 numeral key bit stream.
	KP…	State-synchronised latches for keypress processing.
	KPN	Process a numeral key .
	KPD	Process the decimal point key.
	KPR	Process the recall key.
	KPO	Process an operation key.
	KC, KCE	Clear keys.
	KT, KK	Tally & constant switches.
Control	STn	Primary states of the control state machine.
	NSTn	Next state for the state machine.
	STSUP	Signal to suppress duplicate states in a few instances.
	OPAS	Add/Subtract operation to be performed.
	OPMD	Multiply/divide operation to be performed.
	OPAM	Add/Multiply.
	OPSD	Subract/Divide.
	OPM	Multiply operation.
	OPD	Divide operation.
	OPE	Equals operation.
	OPEA, OPES	Distinguish equal-add from equal-subtract operations.
	FKOP	Flag indicating a constant-operand has been entered.
	ERR	Latched error or overflow state.
	NO12SINCE11	State 12 has not been executed since the most recent execution of State11.
	FDAT	Flag catching conditions within the number cycle.
Sign Flags	SND	Sign of the displayed operand.
	SNO	Sign of the other operand.
	SNM	Sign of the memory / tally register.
Counters	PLC	Primary loop counter for multiply & divide.
	DPD	Displayed decimal point counter.
	DPK	Constant-operand decimal point counter.
	FDP	Flag indicating in time the current digit of the displayed register is fractional (right side of the DP) .
	FDPAL	Flag indicating number has been aligned to the DP switch setting.
Registers	RX	X register bitstream.
	RY	Y register bitstream.
	RM	Memory / tally register bitstream.
Arithmetic	A	A input to Arithmetic Unit.
	B	B input to AU.
	B–A	Perform B–A rather than B+A.
	SUM	Bitstream output of sum from AU.
	N1,2,4,8	A digit passing through the AU, BCD bits for numeral to be displayed.
	N=0	The 4 bits of N are zero.
	NE=10	Early indication N is 10: in the next bit period N will equal 10.
	TC	Ten's carry from add/subtract on digit.

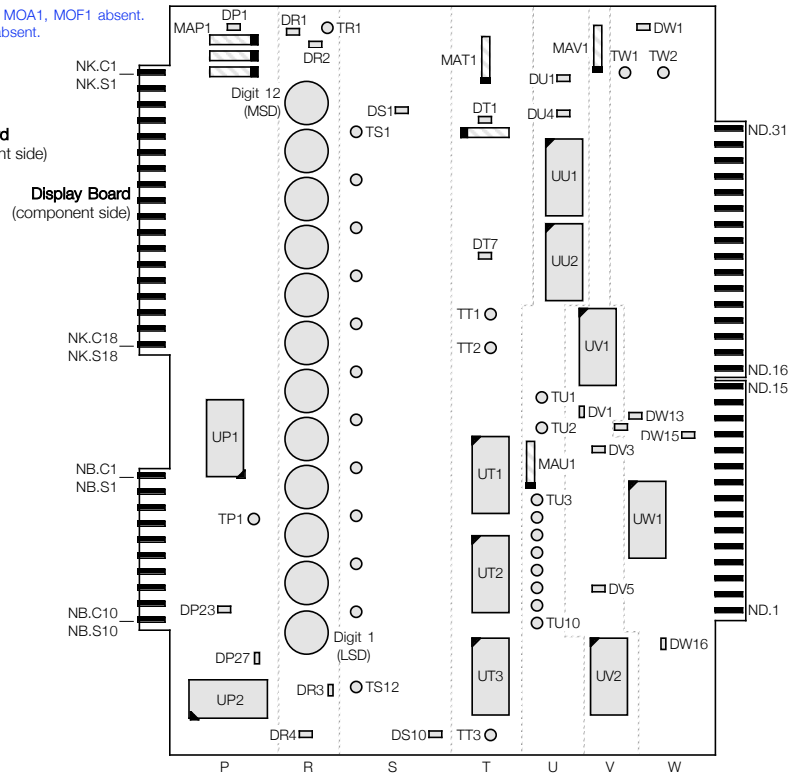
- A "~" in a signal name indicates the logical NOT operation.
- The character "•" in a signal name indicates the logical AND operation.
- The character "+" in a signal name indicates the logical OR operation.



#J: DA23, MOA1, MOF1 absent.
#S: DA7 absent.

Main Board
(component side)

Display Board
(component side)



Component Identification & Location

Components are identified by labels of the form:

<type><alpha><number>

<type> = U IC
D Diode
MA Diode Module And (P, common anode)
MO Diode Module Or (N, common cathode)
T Transistor.

<alpha> = Main board: row T–>B
Display board: column L–>R)

On the Main board, ICs are located in a fixed grid:
<number> = 1..7 (L–>R)

For other Main board components:
<number> = 1..last (enumeration L–>R)

On the Display board, for both ICs & other components:
<number> = 1..last (enumeration T–>B)

Left, Right, Top, Bottom relative to the board orientations shown.

NA,B	S	C	
K00~	1	1	KPD~
ØD13~	2	2	ØDPS~
OPSD~	3	3	KT~
KRND~	4	4	OPMD~
OPAS~	5	5	FKOP
POC~	6	6	ØD16
ST12~	7	7	V–24
OPEA~	8	8	KPO~
ST31~	9	9	OPES~
KPO	10	10	FKOP~

NK	S	C	
GND	1	1	K1~
K3~	2	2	V–N
K2~	3	3	FIL2
K4~	4	4	K6~
K8~	5	5	K9~
K0~	6	6	V–D
K00~	7	7	KES~
K7~	8	8	KEA~
K5~	9	9	KA~
KRND~	10	10	KC~
FIL1	11	11	KT~
KCOM	12	12	KP~
V–24	13	13	KS~
ØD3~	14	14	KM~
ØD1~	15	15	KD~
ØD5~	16	16	ØD4~
KR~	17	17	KCE~
ØDPS~	18	18	KK~

ND

N1	15	ST34~	31
ØD16~	14	ST11~	30
GND	13	ØEOD~	29
DPD~	12	KC~	28
KPR~	11	ERR~	27
ØB8~	10	KPN	26
ØD12~	9	OPAM~	25
ØD0~	8	KPN~	24
ØD15~	7	KCE~	23
ØD1~	6	ØB4~	22
OPE~	5	DISPON	21
ØB1~	4	NEG~	20
N2	3	ØB8	19
N4	2	ØC	18
N8	1	ØB2~	17
		ØT	16

TEAL: IME 41
Calculator

Section: Connectors & Board Layout
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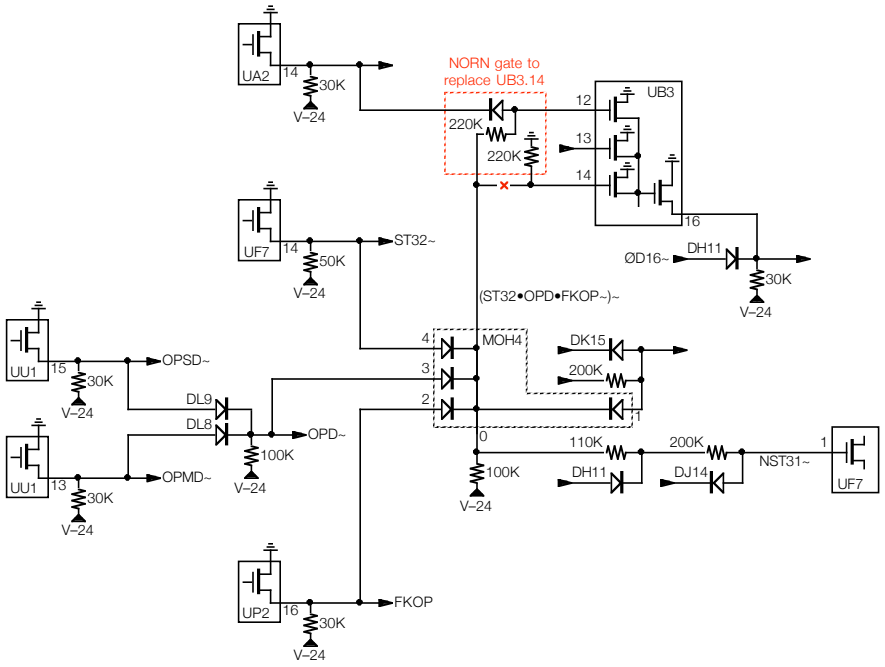
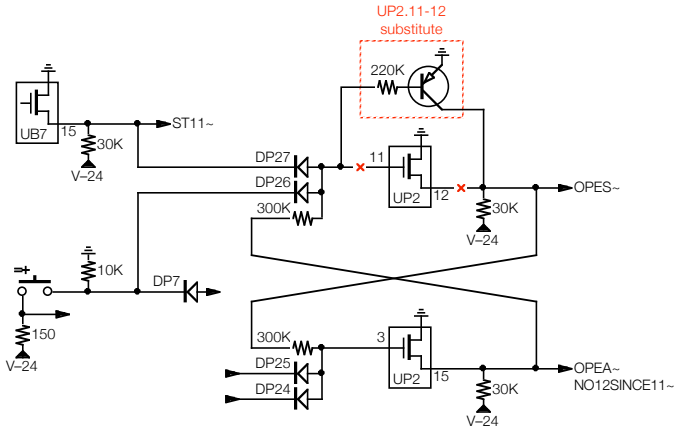


#J Unit - Fix for Bad UB3.14 Input

3-input NORN gate in UB3 is extended with a passive 2-input NORN gate to pin 12 to replace the bad input at pin 14.



#S Unit - Fix for Bad UP2.11-12 Inverter

Replacement for failed MOSFET inverter. If output does not go adequately HIGH, try:

- reduce 220K base R to 100K.
- use 2 transistors in Darlington configuration.