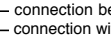
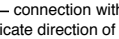
Monroe 925 Calculator

Contents

This is not the manufacturer's schematic.
This data has been derived through the reverse engineering of a physical unit.

B. Hilpert
1997 Dec

Notes

- The symol  denotes a physical connector pin, where *c*=connector, *pp*=pin and *s*=side (T=top, B=bottom). Solid black end is the male side of the connector. White end is the female side of the connector.
-  connection between different sections.
   connection within same section.
  Arrows indicate direction of signal or energy flow.
- The symbol denotes Vcc.
- Capacitance in microfarads unless otherwise indicated.
- The delay line memory transducers are based on magnetostrictive principles. See the article “Magnetostrictive Delay Lines” in “Electronics World”, Jan. 1964.
- These drawings based on unit with Serial No.: E017715. These drawings are presumed to also apply to the Monroe 920 and the Canon 1210. The Monroe 920 does not provide the accumulator functions, the Canon 1210 has 12 rather than 13 displayed digits.
- See EEC pages at madrona.ca for additional information.

Log

- 1997 Dec: Initial drawing / bhilpert.
- 2000 Oct: Symbol names changed to Ø standard.
- 2005 Jan: Memory organisation and timing details added. Some other symbol name changes, some reorganisation of arithmetic page.
- 2023 Dec: State diagram added, copied from old simulation.

Sections and Signal Names

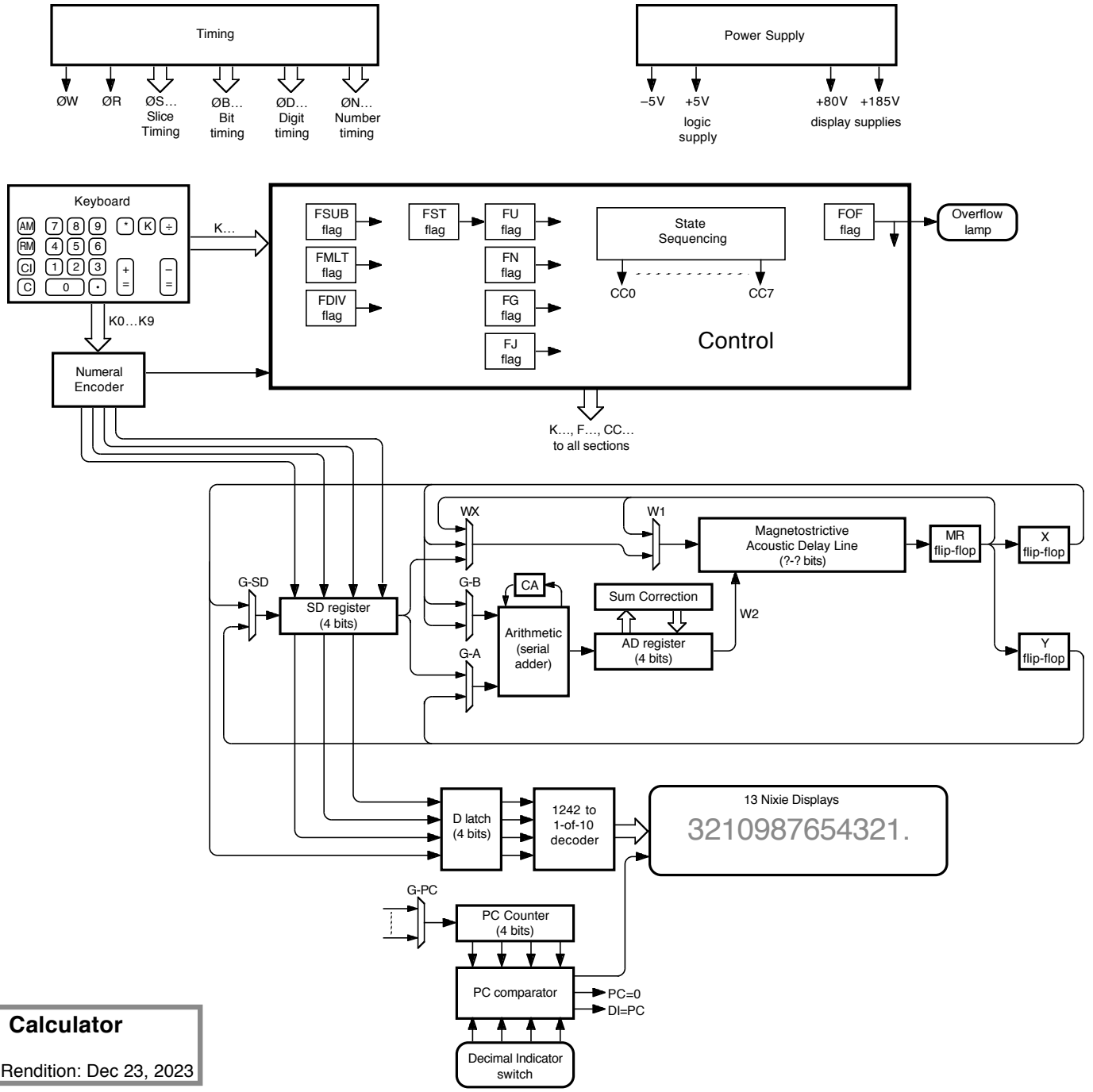
Section	Signal	Description
Timing	ØW	1 Mhz clock pulse. Used for injecting pulses into the acoustic delay line.
	ØR	500KHz clock pulse. This is the slice clock.
	ØS0	100KHz clock pulse with 1/5 duty cycle. This is the basic bit clock. The bit period is divided into 5 slices. The slices are used for interleaving the bits of the registers within one bit period.
	ØS4	Bit Slice 4.
	ØB0,3	Bit clock periods.
	ØD0..15	Digit clock periods. There are 16 digit periods. Bits of the displayed digits are contained in periods 0 to 12 and displayed during periods 1 to 13.
	ØN0..3	4 number cycles. Each number cycle is a complete cycle of the 16 digits.
Keyboard	K…	The keyboard and numeral encoder.
	SUB	Subtract operation.
	MLT	Multiply operation pending.
	DIV	Divide operation pending.
	MD	Multiply or Divide operation active.
	FU	Key-pressed flag to initiate operation execution, synchronised to state timing.
Control	CC0…CC7	The 8 states of the operation execution state machine.
	FN	Flag to indicate ‘within’ number during entry, 1 after first digit of number has been entered.
	FG	A flag to modify state actions during some operations.
	FJ	Data-state capture flag. Also used to indicate whether decimal point has been entered during number entry.
	FOF	Overflow Flag.
	CD…	Assorted derived control signals to various sections.
Memory	X	X register bit stream from the memory.
	Y	Y,A,B and C register bit streams from the memory.
	SD…	A 4-bit register used for shifting, numeral entry and display update.
	MOF	Overflow indication from the X register to the overlow flag.
Arithmetic	AD	Bit stream output from arithmetic, after sum correction.
	ACA	Carry from arithmetic.
	FCA	Carry Flag.
PC Counter	PC=0	1 when the decimal point counter is 0.
	DL=PC	1 when the decimal point counter coincides with the switch-selected decimal location.
	DP	Decimal point from counter to display.

A lowercase “n” in a symbol name indicates the logical NOT operation.

Original Signal Names

Some signal have been renamed from those names printed on the printed circuit boards:

Board/Original	Schematic	Board/Original	Schematic
CPR	ØR	n(KP•FN)	nKPFN
CPW	ØW	KN+KP	KNP
nCP	ØS0 (note inversion)	n(KC+KCl)	nKCE
TS4	ØS4	KA+KS	KAS
TBx	ØBx	M+D	MD
TDx	ØDx		
nTD12-14	nØD1314	SD1	SD4
SCTx	ØNx	ECP	nLDSDK



Monroe 925 Calculator

Section: Block Diagram

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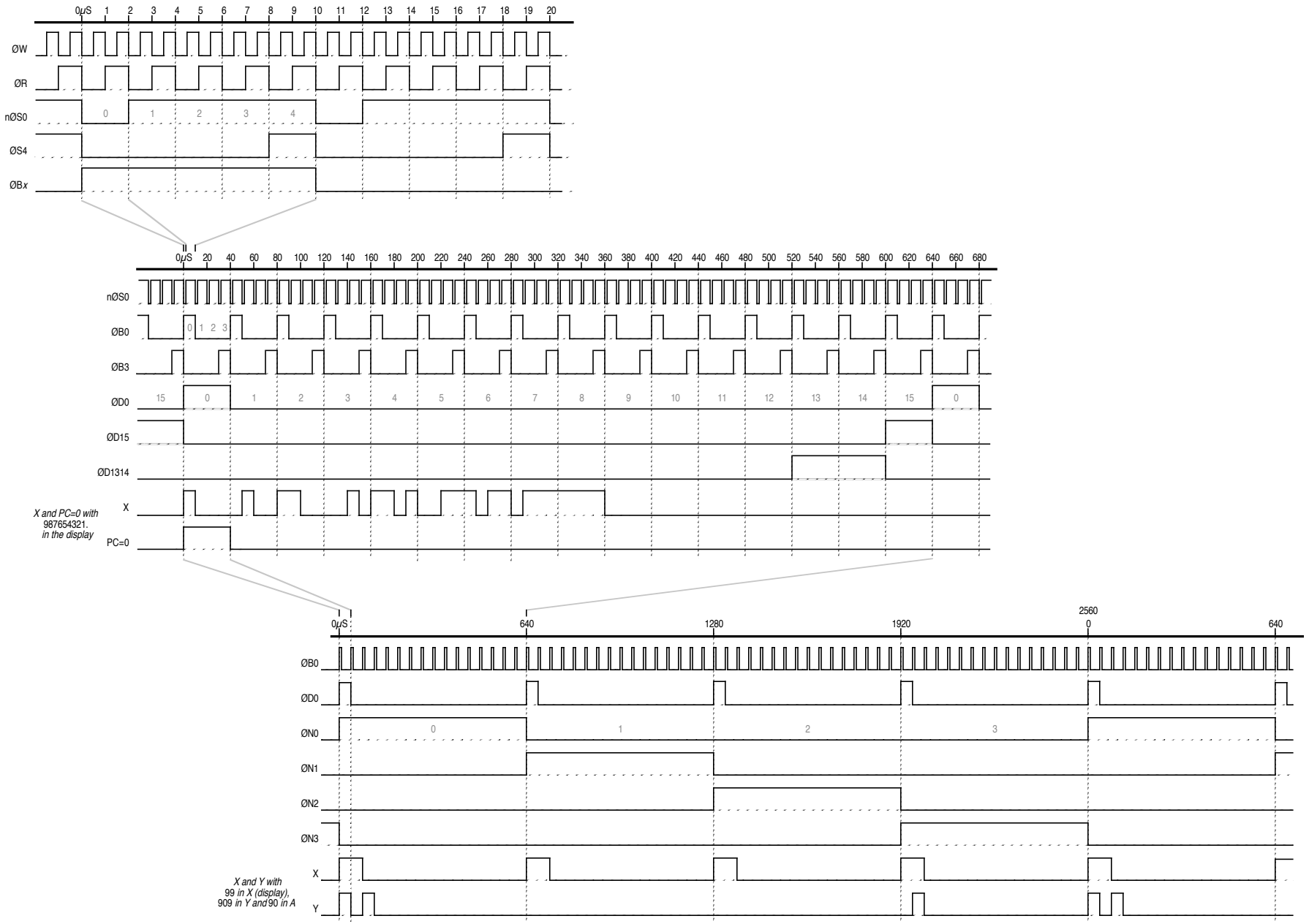

Monroe 925 Calculator

Section: Timing Diagram

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Memory Organisation

The Monroe 925 incorporates 5 registers for storage of numbers, each of 16 decimal digits. The decimal digits are encoded using 1242 bit weighting (figure 1), rather than 1248. The second 2 bit is referred to here as the W bit (tWo) to distinguish it from the first 2 bit. The 5 registers are:

Register	Use	Period
X	displayed operand	ØN0,1,2,3
Y	2nd operand	ØN0
C	temporary (product,dividend)	ØN1
B	temporary (quotient)	ØN2
A	user memory / accumulator	ØN3

The 5 registers present a requirement for 5•16•4=320 bits of storage. The magnetostrictive acoustic delay line and a few flip-flops provide the storage for these registers. The method of achieving this storage in a single delay line is relatively sophisticated, so this discussion will start with higher-level functional representations of the storage.

Figure 2 presents a representation of the storage as seen at the register-bit level. The X register cycles through the shift register ADLX and flip-flop X, totalling 16*4=64 bits. The Y, A, B and C registers cycle sequentially through ADLY, Y and the 4 AD flip-flops, totalling 4*16*4=256 bits. As a number is 64 bits long, Y, A, B and C only cycle once every 4 number cycles while the X register cycles every number cycle. Consequently operations can be performed between the X register and any of Y, A, B, and C by choosing the appropriate number cycle period (ØN) during which to execute the operation (see table above).

To provide this storage in a single delay line the register bits are interleaved by 'slicing' the period of each register-bit (ØBn) into 5 shorter periods (ØSn) and storing a bit of each of the 5 registers in each of the 5 bit-slices. A given register is written into the delay line during one of the 5 slice periods and read out by being clocked into the X or Y flip-flop during particular slice periods. The data persists in the X and Y flip-flops for an entire register-bit period. This is shown functionally in figure 3.

A neat trick is performed at this point in the design to achieve the sequencing of the Y, A, B, and C registers. The delay line length including the M and MR flip-flops is one slice short of a full number period. Bits of the X register enter the delay line during slice ØS0 and show up in the M flip-flop during slice ØS4. They are resynchronised to the number cycle during the longer stay in the X flip-flop. Bits of the Y, A, B and C registers initially enter the delay line during slice ØS4. The bits then re-enter the delay line three more times before heading for the Y flip-flop. As a result of the delay being one slice short, each re-entry is one slice earlier than the previous entry and a particular bit only appears in the Y flip-flop during one of the four ØN periods. The 'slippage' of a data bit is halted when the bit is resynchronised to the number cycle during the longer stay in the Y flip-flop.

Figure 4 presents a more complete representation of the contents of the acoustic delay line memory and the flip-flops in the register bit paths during the normal or idle state. Each 1-bit storage element is labeled with the data bit contained in that element just before the end of the slice period ØS2 during the second bit (ØB1) of the first digit (ØD0) of the number cycle during which the X and Y registers are processed (ØN0).

Figure 4 exemplifies how the sequence of the Y, A, B, C register bit-slices shifts in the delay line relative to that of X between ØN cycles. The sequence of the register slices during period ØN0 is apparent at the right end of the delay line (XYCBA). At the left end of the delay line bits have been injected which will emerge during ØN1, but now the sequence is XCBAY (the Y bits will be injected into the empty bit-slice slots by the W2 write head). In subsequent number cycles the slice sequence will be XBAYC, XAYCB before repeating.

The delay line provides for storage of 317.5 bits. 4 bits are not utilised (shown in figure 4 as empty bit slots), leaving 313.5 bits utilised. The M, MR, X, Y and 4 AD flip-flops of the arithmetic sum correction are also part of the register storage, for a total of 321.5 bits.The extra 1.5 bits are accounted for by overlap in time of data in flip-flops and in the delay line. In figure 4 bits X02 and B02 are simultaneously in a flip-flop and the delay line.

Each bit-slice occupies 2 μS in the delay line, if the value of that bit is 1 then a 0.5μS pulse is injected into the line during that 2μS interval.

Figure 1: Decimal Value Encoding

Value	W421
0	0000
1	0001
2	0010
3	0011
4	0100
5	1011
6	1100
7	1101
8	1110
9	1111

Figure 5: Some Characteristics of the Delay Line

Bits:	317.5		
Total Delay & Length:	635 μS	74 inches	1880 mm
Bit-slice:	2 μS	0.23 inches	5.9 mm
Slice-pulse:	0.5 μS	0.058 inches	1.5 mm
Velocity:		0.12 in/μS	3.0 mm/μS
Velocity:		6600 mi/H	10700 Km/H

Figure 2: Register-bit-level Representation of the Delay Line Storage

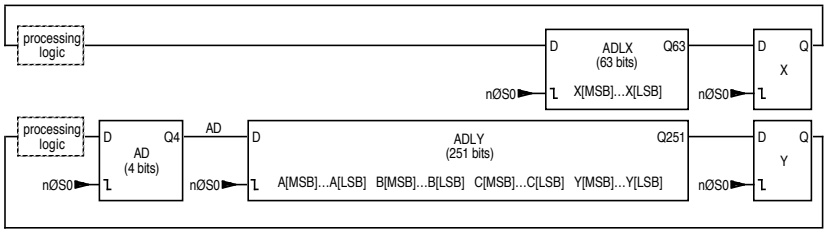


Figure 3: Slice-level Representation of the Delay Line Storage

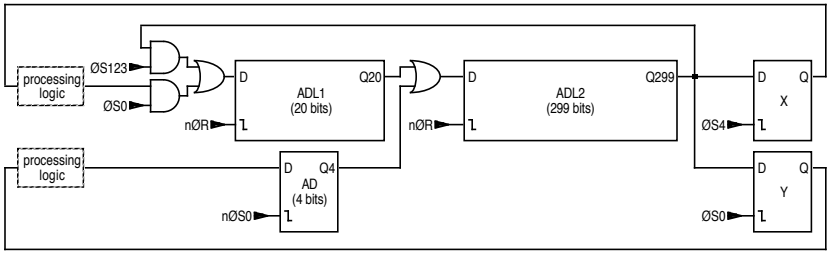


Figure 4: Acoustic Delay Line Storage and Idle-State Bit Paths
- before end of period ØN0-ØD0-ØB1-ØS2 -

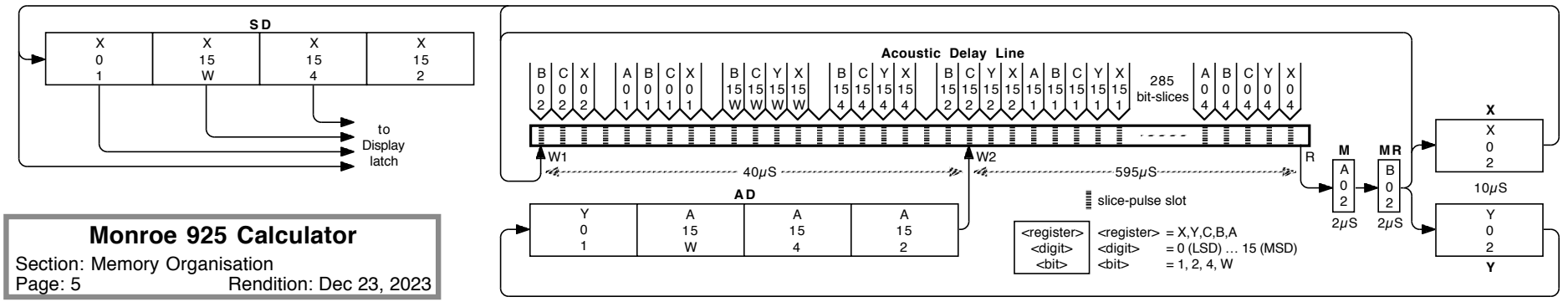


Figure 6: Acoustic Delay Line Timing

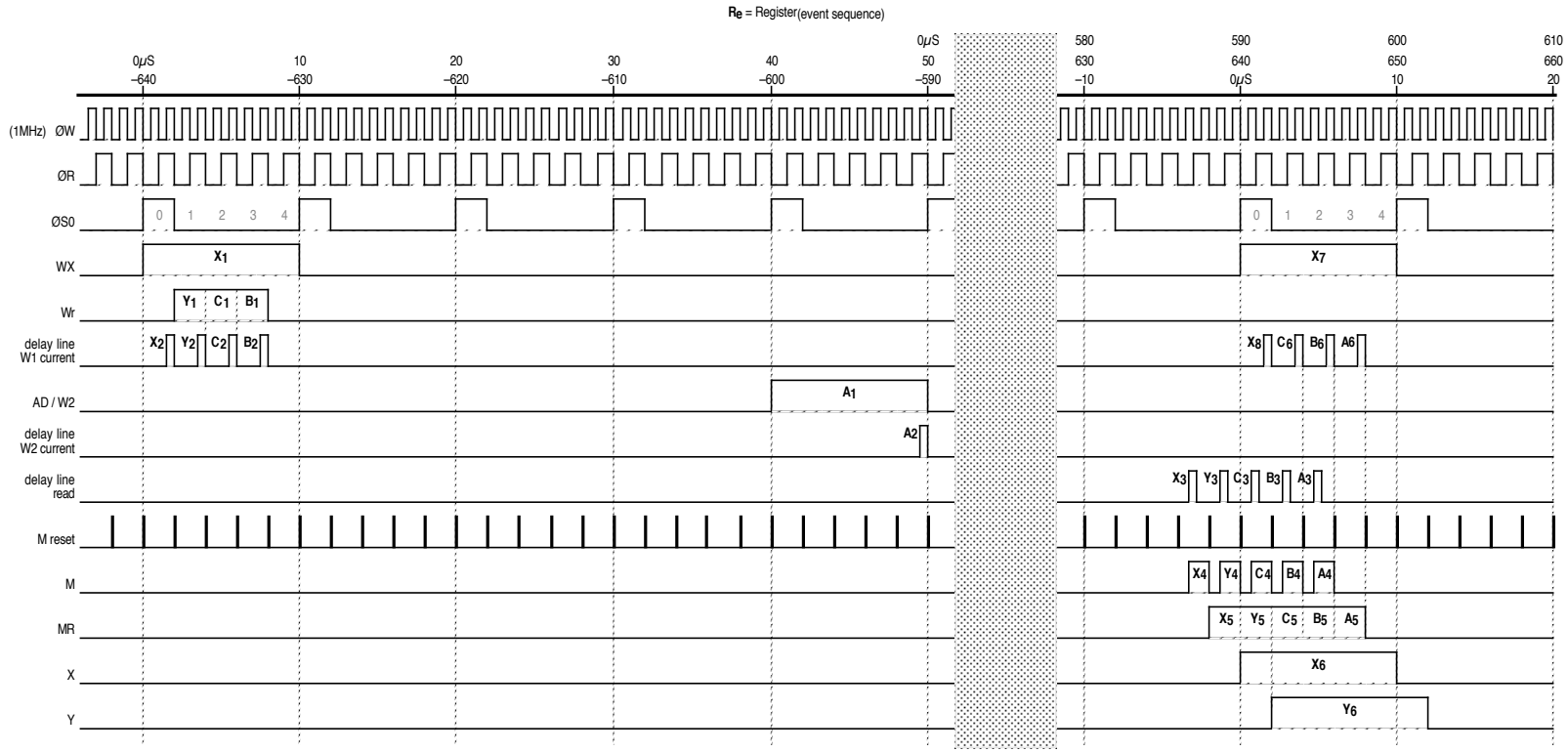


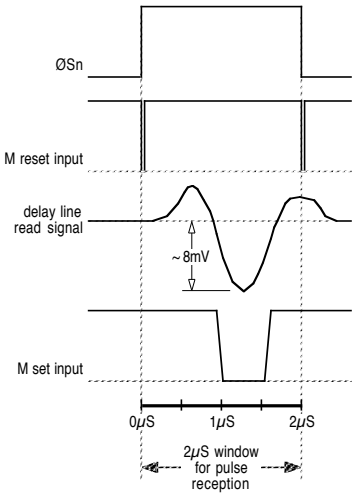
Figure 6 presents the timing for data bits injected into the delay line. Shown is one data bit of each register being written into the delay line and the trail of events each bit produces to the point it is cycled back into the line.

A bit of the X register at the WX input (X1) produces current in the W1 write coil (X2) during ØS0 to inject a pulse at the beginning of the delay line. When this pulse has traversed the delay line it produces a read pulse (X3) which sets the M flip-flop (X4) and is then transferred to the MR flip-flop (X5). At the end of ØS4 it is clocked into the X flip-flop (X6) where it persists for an entire register-bit period and is available for register-level operations. If appropriate to the operation it is injected back into the delay line (X7,X8), again during ØS0.

For the Y, A, B, and C registers a data bit initially enters the delay line during ØS4 via the W2 write head. Shown is a data bit from the A register starting it's cycle (A1,A2). It exits the delay line (A3), is transferred to M and then MR (A4,A5) and is written back out via the W1 head (A6), but now one slice earlier. In subsequent number cycles it follows the sequence of the other register bits (Bn,Cn,Yn) until finally entering the Y flip-flop after 4 number cycles. From the Y flip-flop it shifts through the 4 AD flip-flops, with appropriate register-level operations being performed, before being injected back into the delay line via W2.

As shown in figure 7, a bit pulse exiting the delay line must do so within a 2μS window to set the M flip-flop during the appropriate bit-slice period. The entire 0.5 μS pulse (actually slightly wider after traversing the delay line) must be within the 2μS window to avoid triggerring the M flip-flop inappropriately. The longer W1 delay is centered around 635μS (measured 635.5). The shorter W2 delay is centered around 595μS (measured 595.5).

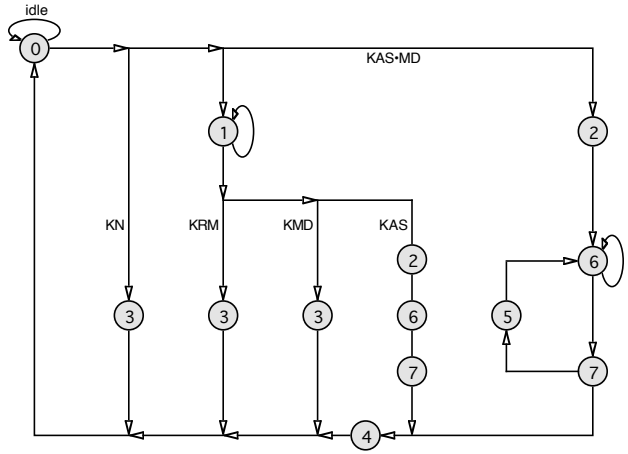
Figure 7: Delay Line Read Timing

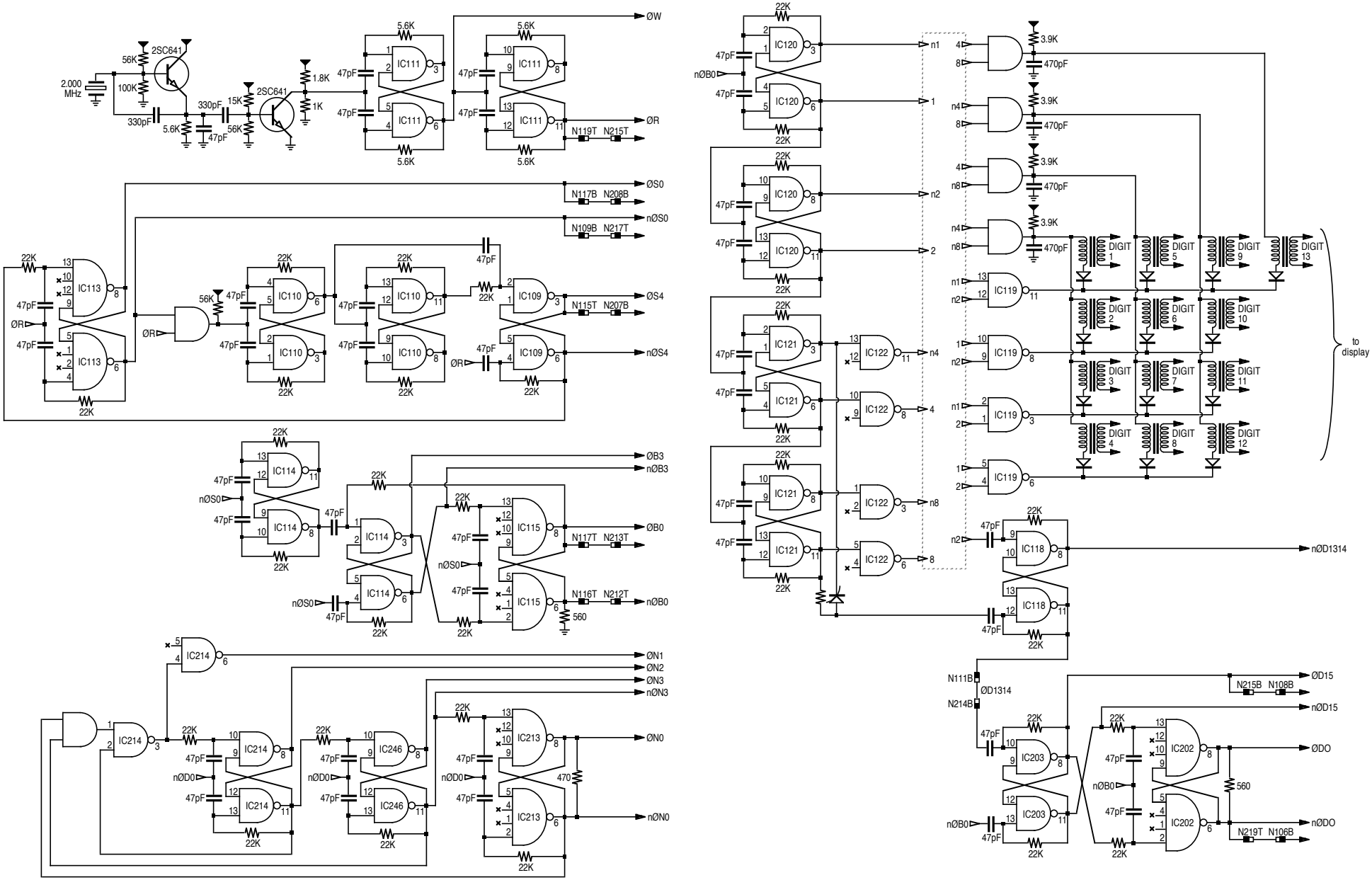


State Diagram

Lines represent state transitions occuring at the end of a full number cycle.

State	Actions
1	Shift X left till aligned with selected DP
2 - KAS	?
2 - Mul,Div	Swap X <–> Y
3 - KN:	Shift X left, KN–>X[LSD]
3 - KRM	Copy A –> X
3 - KMD	Copy X –> Y
4 - Add	Copy Y –> X
4 - Mul,Div	X–>Y, B–>X, if KAM: A+X–>A
5	Shift Y, B & C left as unit
6 - KAS	If KAM: A±X–>A
6 - Mul	--Y[MSD], if no borrow C+X–>C
6 - Div	C-X–>C, ++B[LSD]
7 - KAS	Y±X–>Y
7 - Mul	Cear or ++ Y[MSD]
7 - Div	C+X–>C (restore)





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Section: Timing

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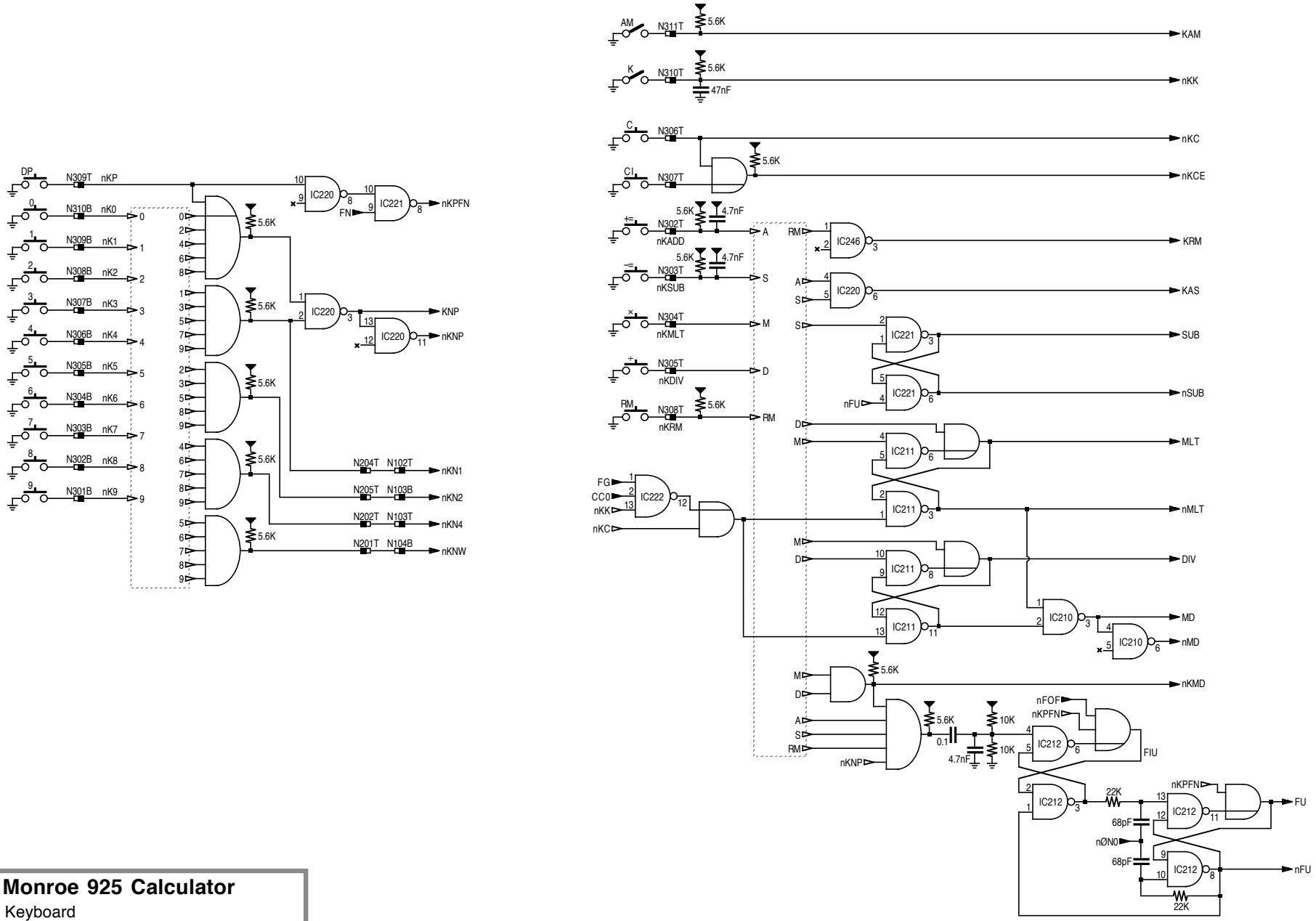

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Section: Keyboard

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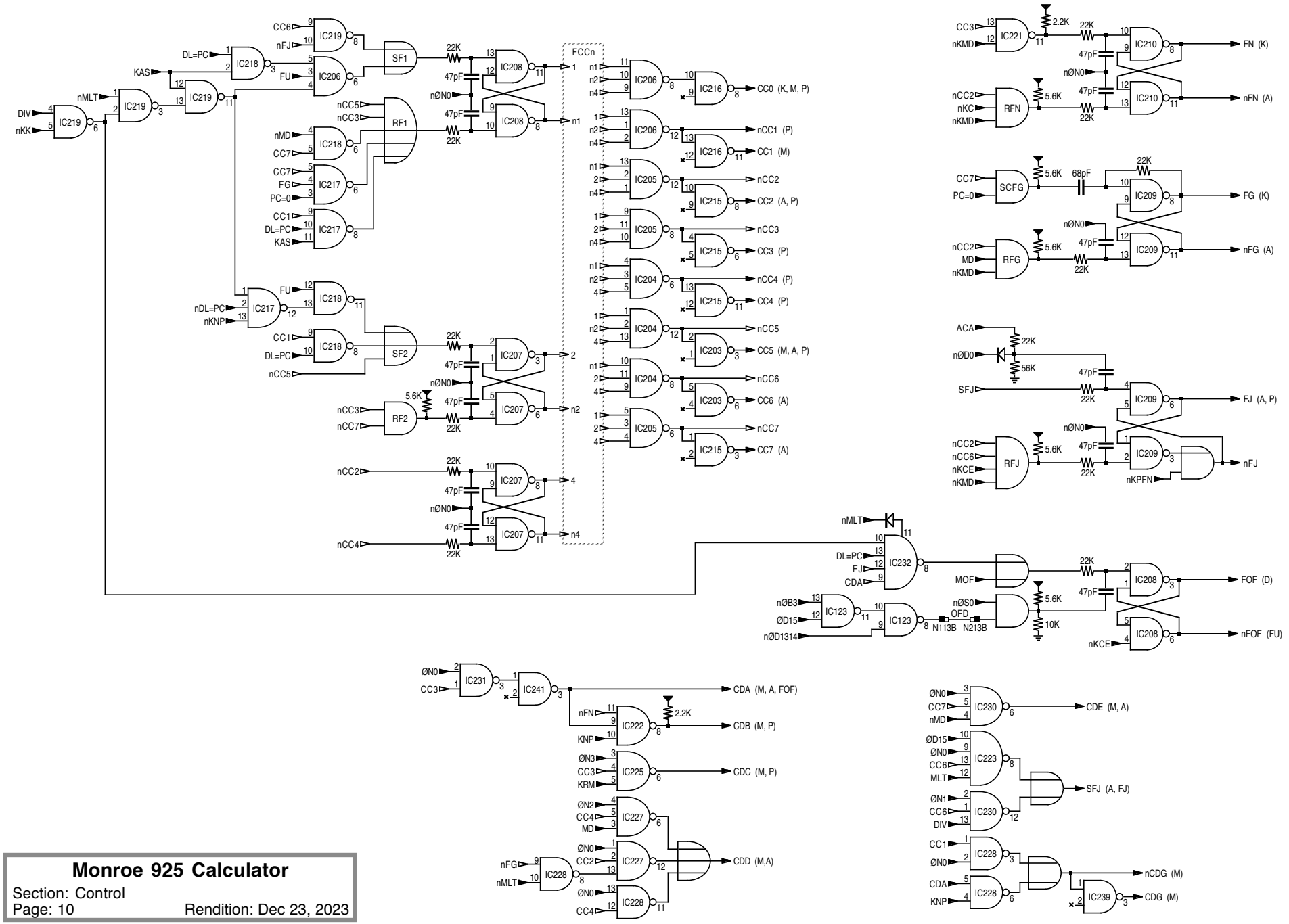

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Section: Control

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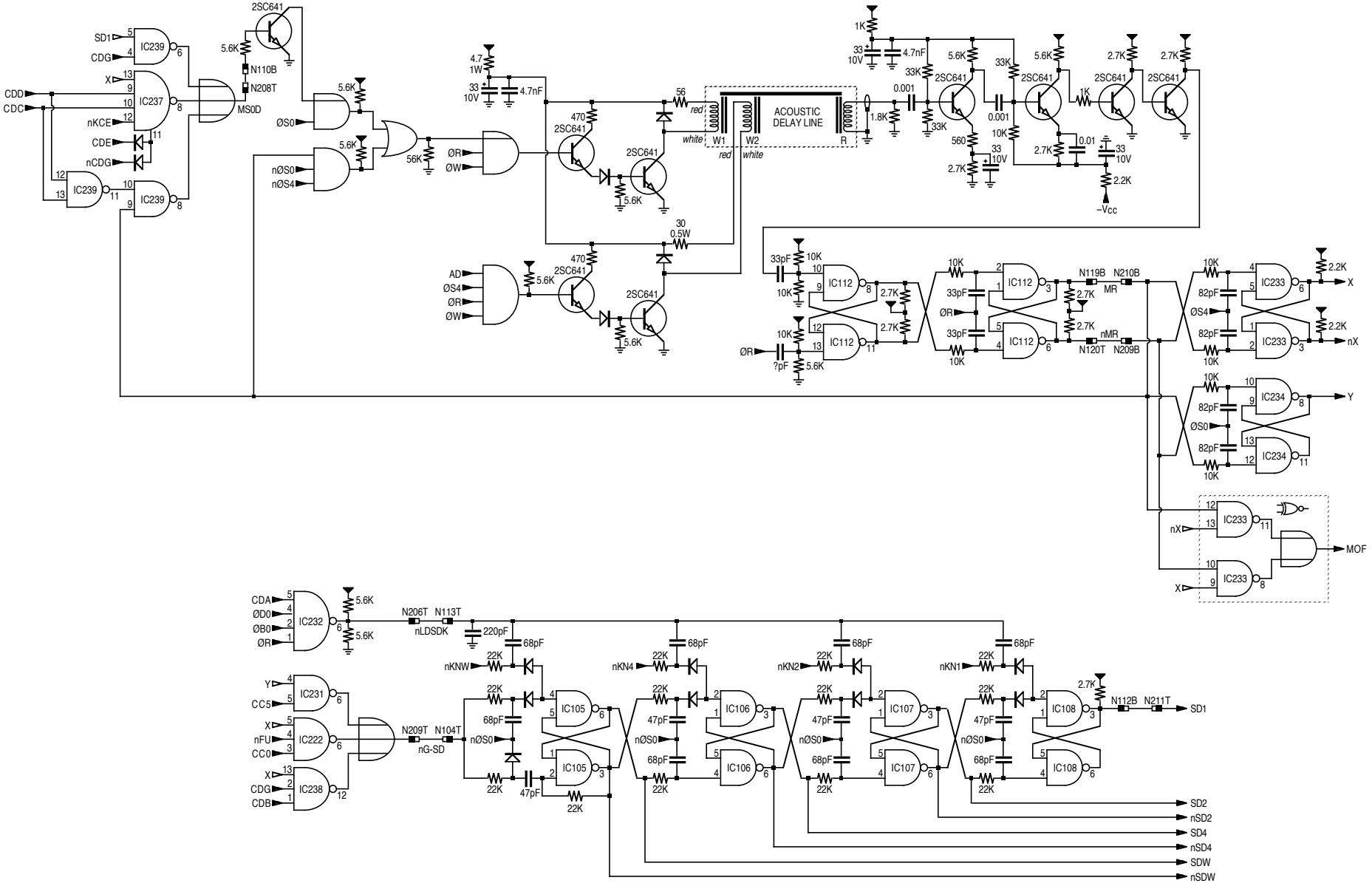

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Section: Memory

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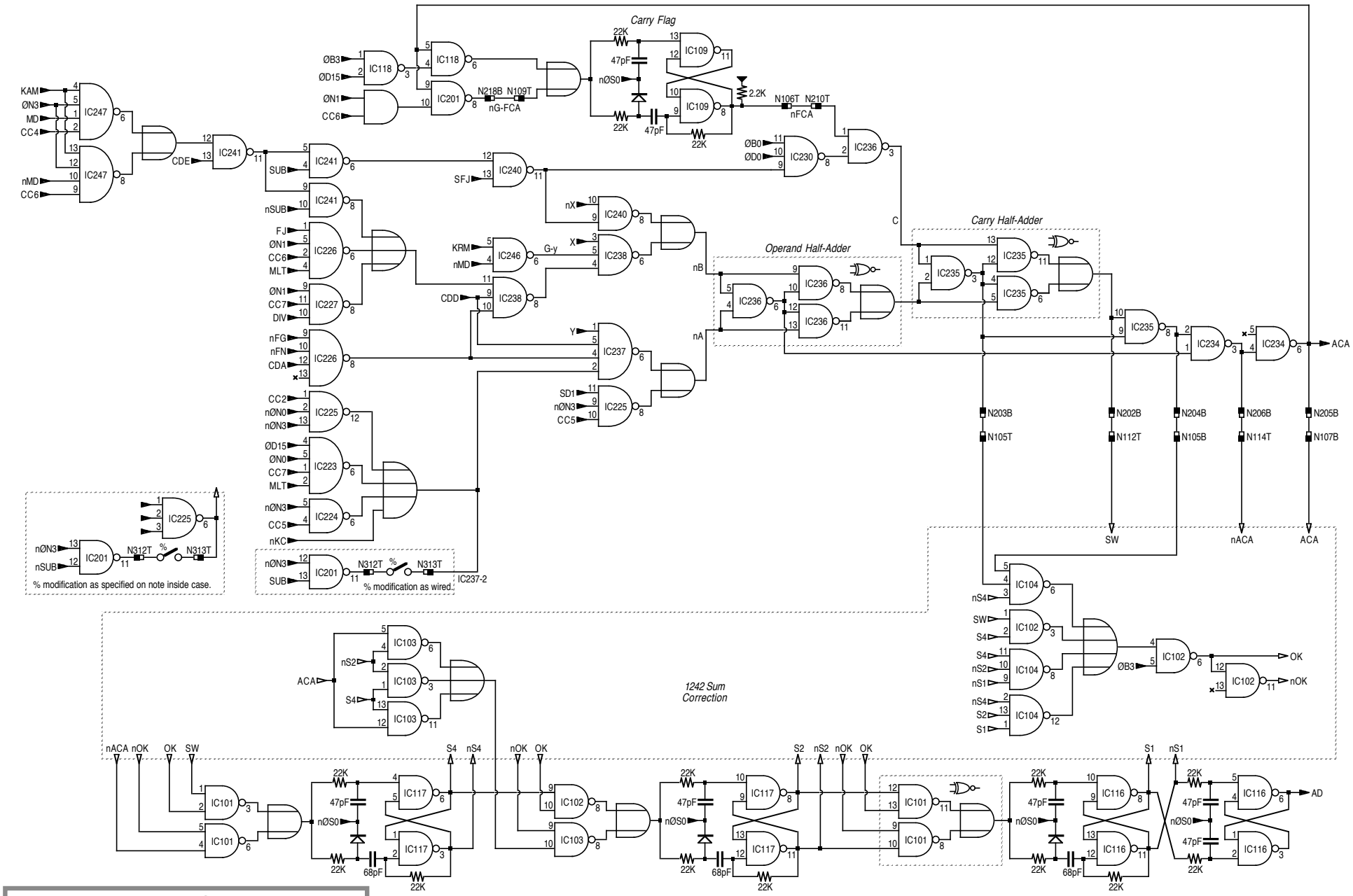

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Section: Arithmetic

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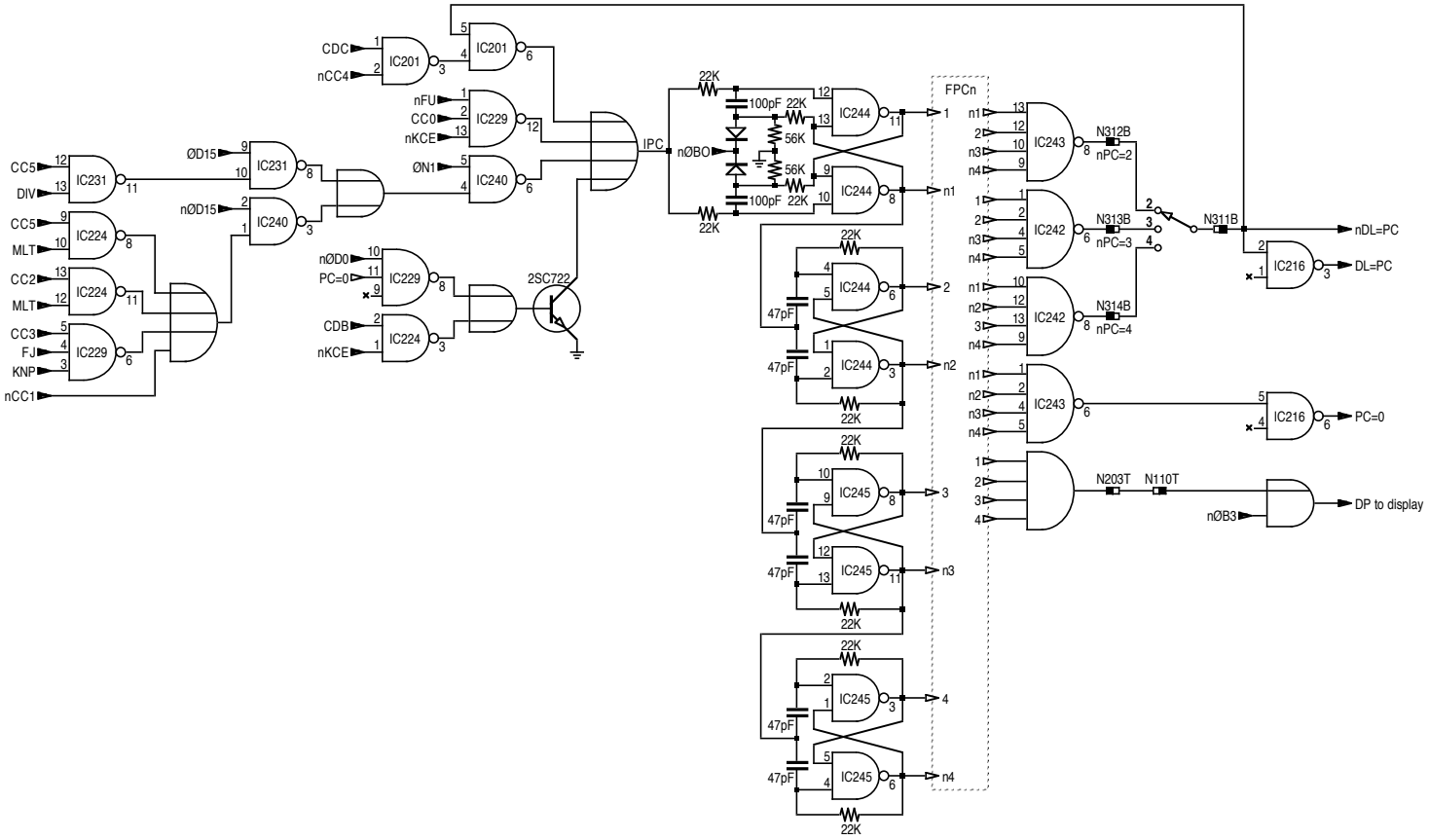

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Section: Decimal Point Counter

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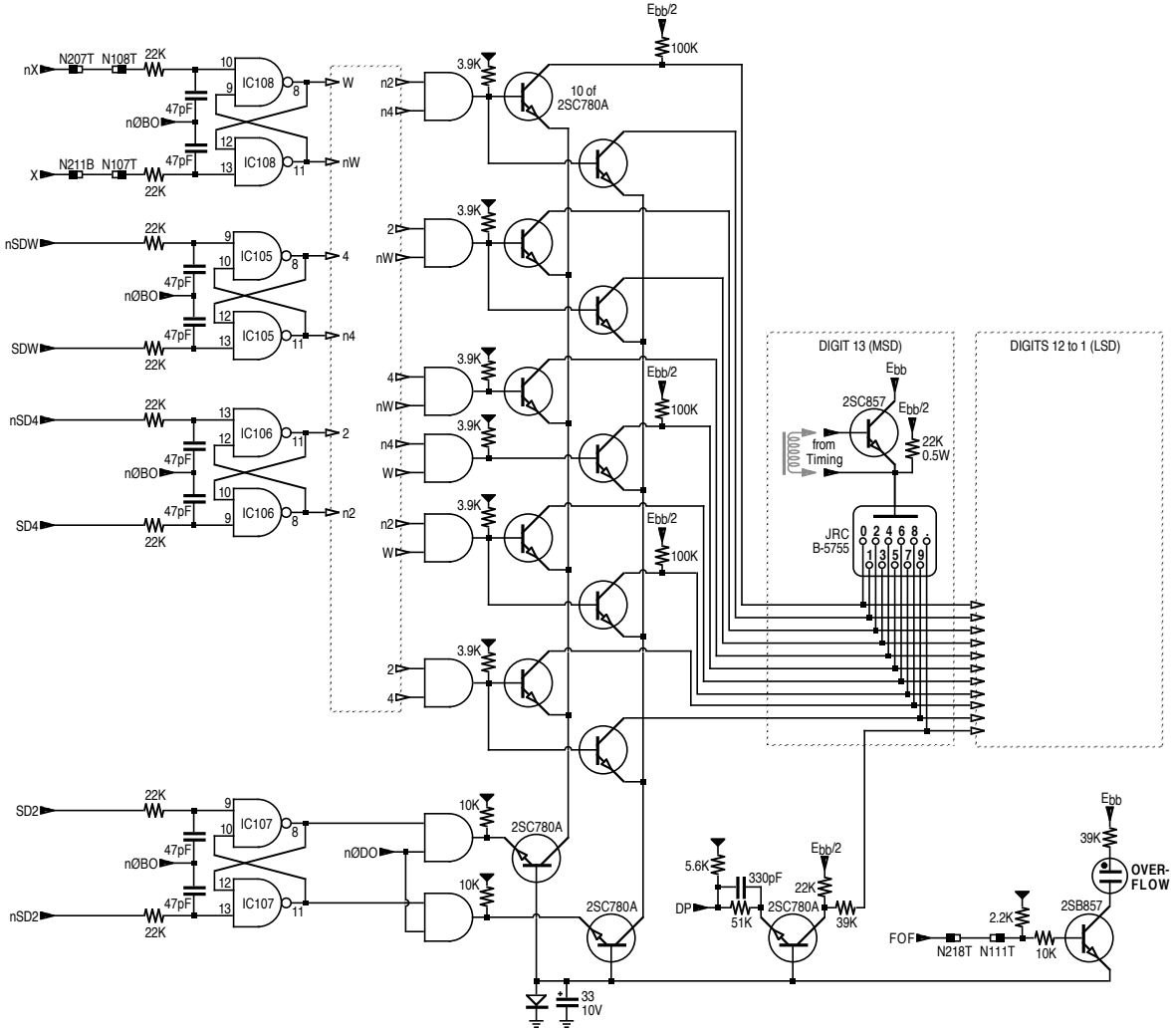

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Section: Display

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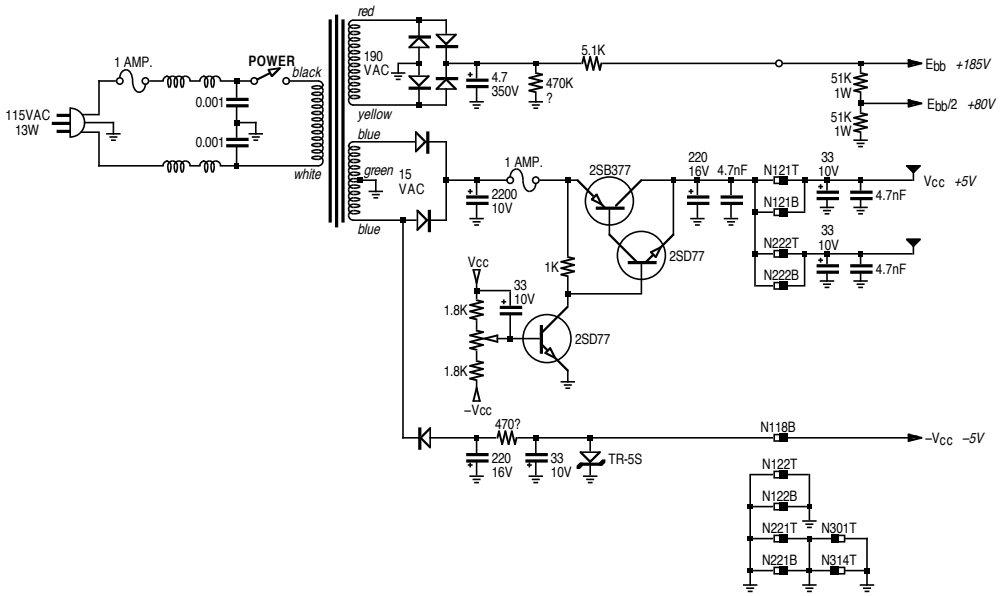
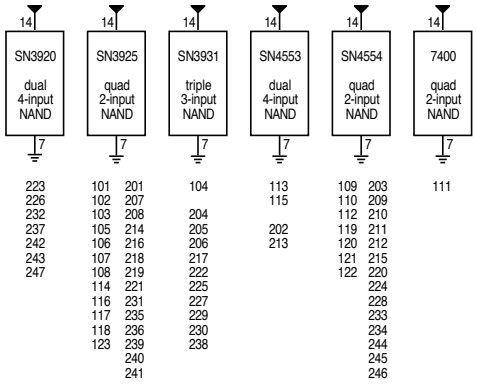
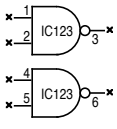




Unused Gates



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Section: Power Supply

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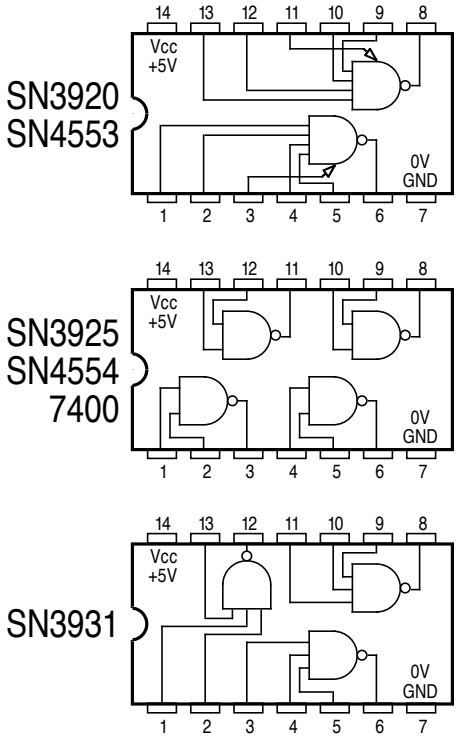
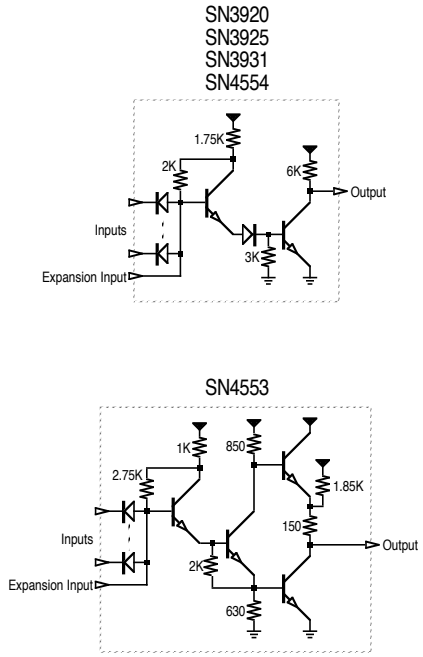
SN3900 / 4500 Series DTL
IC Pinouts

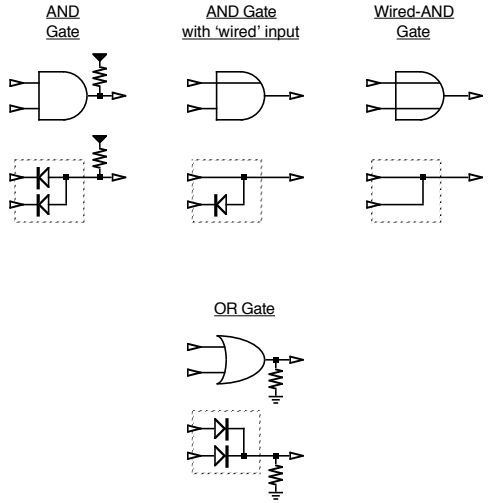


SN3900 / 4500 Series DTL
Gate Construction

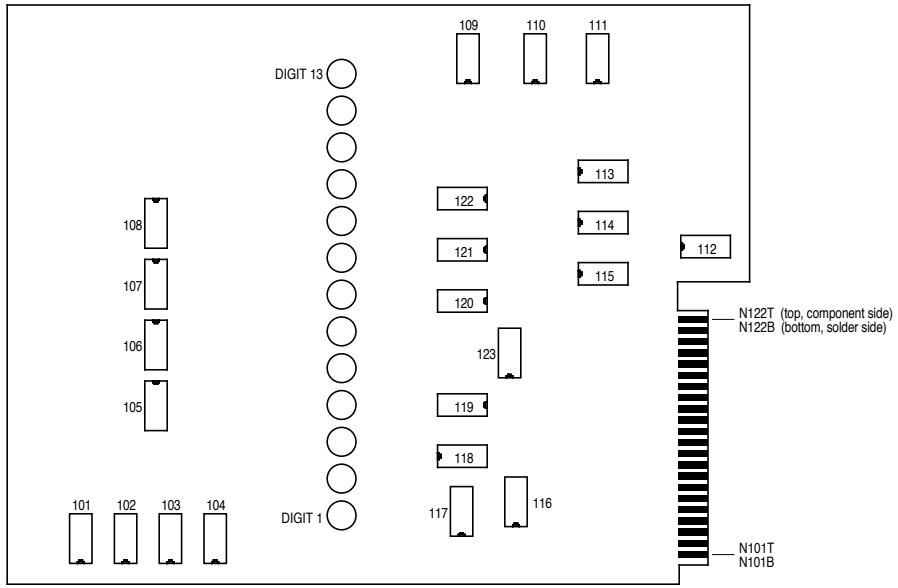


Discrete Gate Construction

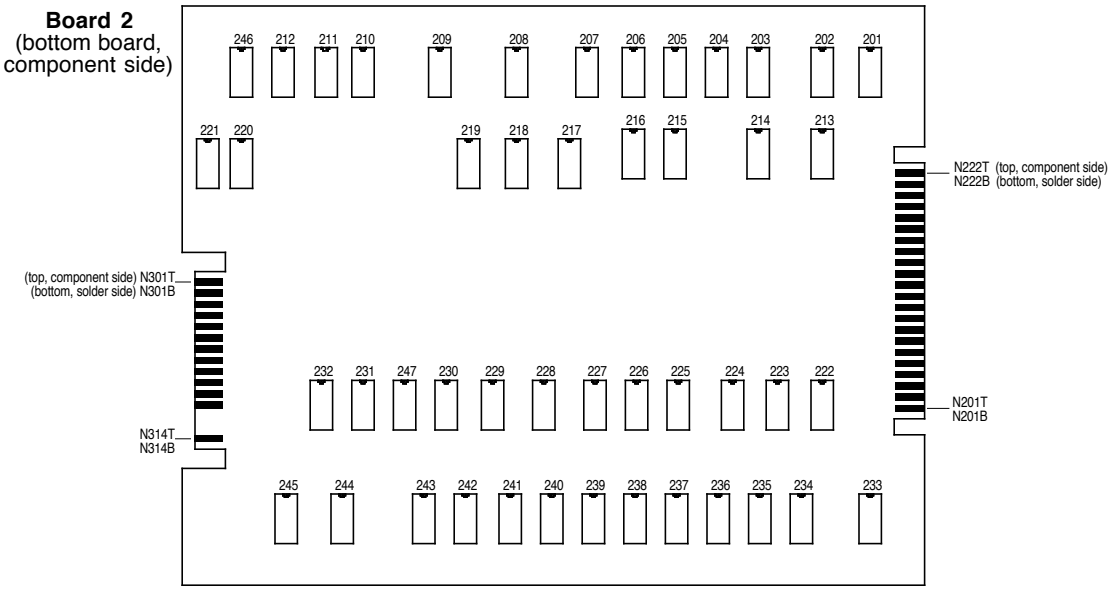
A few gates are constructed from discrete diodes and resistors. The internal construction of these gates is shown in the following diagrams. A wire–AND construction is indicated by the input line traversing the width of the gate.



Board 1
(top board,
component side)



Board 2
(bottom board,
component side)



N1

	T	B	
GND	22	22	GND
Vcc	21	21	Vcc
nMR	20	20	-
ØR	19	19	**MR**
-	18	18	–Vcc
ØB0	17	17	**ØS0**
nØB0	16	16	-
ØS4	15	15	-
nACA	14	14	-
nLDSDK	13	13	**OFD**
SW	12	12	**SD1**
FOF	11	11	**ØD1314**
DP	10	10	MS0D
nG-FCA	9	9	**nØS0**
nX	8	8	nØD15
X	7	7	ACA
nFCA	6	6	nØD0
IC235-3 (A)	5	5	*IC235-8 (A)*
nG-SD	4	4	nKNW
nKN4	3	3	nKN2
nKN1	2	2	-
-	1	1	-

N2

	T	B	
Vcc	22	22	Vcc
GND	21	21	GND
-	20	20	-
nØD0	19	19	-
FOF	18	18	**nG-FCA**
nØS0	17	17	-
-	16	16	-
ØR	15	15	**nØD15**
-	14	14	ØD1314
ØB0	13	13	OFD
nØB0	12	12	-
SD1	11	11	**X**
nFCA	10	10	MR
nG-SD	9	9	nMR
MS0D	8	8	ØS0
nX	7	7	ØS4
nLDSDK	6	6	**nACA**
nKN2	5	5	**ACA**
nKN1	4	4	***IC235-8 (A)***
DP	3	3	***IC235-3 (A)***
nKN4	2	2	**SW**
nKNW	1	1	-

• Bold-faced expressions are signal sources.

N3

	B	T	
nK1	1	1	GND
nK2	2	2	nKADD
nK3	3	3	nKSUB
nK4	4	4	nKMLT
nK5	5	5	nKDIV
nK6	6	6	nKC
nK7	7	7	nKCE
nK8	8	8	nKRM
nK9	9	9	nKDP
nK0	10	10	nKK
nDL=PC	11	11	KAM
nPC=2	12	12	-
nPC=3	13	13	-
nPC=4	14	14	GND