Altair 8800b-r Computer

Altair 8800b - Reconstruction

Schematic

Contents

NOTES

- IC locations are identified by a label of the form:
  U<board><alpha>

  <board> = two characters
  FP = Front Panel
  FN = Front Panel Interface

- The symbol —o|o— represents a connector pin. The solid black end is the male side, the white-filled end is the female side.
  Connector pins are identified by a label of the form:
  N <connector> . <pin>

- A small black marker on the upper half of a gate symbol indicates an open-collector output.

- Based on the MITS schematic with alterations for reconstructed interface board.

- 2021 Jun: This drawing / bhilpert.

Implementation differences of reconstructed front panel interface board from original board (function remains the same).

Alterations to avoid peculiarities of 8800b CPU board, allowing operation with the 8800 CPU board.

JUMPERS

FP.A-D:	Slow is 8 / Sec	[8800b.pdf.5-26]
FP.B-D:	Slow is 2 / Sec	
FP.C-D:	Slow is 1 / 2Sec	
FP.E-F	closed: SS/Slow executes an instruction	
	open: SS/Slow executes a machine cycle	
FP.G-H:	Reset is always active	
FP.G-J:	Reset not active when running	
FN.A-B	closed: Data LEDs show IO input data	[8800b.pdf.3-89]
	open: Data LEDs do not show IO input data	
FN.C-D	closed: Data LEDs show IO output data	
	open: Data LEDs do not show IO output data	
FN.E-F	closed: Data LEDs show only IO output data addressed to LEDs (port 377)	
	open: Data LEDs show all IO output data	
FNJX	closed: When running, Data LEDs show last state prior to running, or IO data per jumpers FN.A:.F.	
	open: When running, Data LEDs simply follow S100 DO lines.	
FNJY.1-2	Ready from the front panel drives S100.xRDY.	
FNJY.2-3	Ready from the front panel drives S100.pRDY.	

RATIONAL

This is a schematic for a reconstruction of the Altair 8800b front panel interface board, hereafter referred to as the RIB. The RIB differs from the 8800b interface board in gate organisation and physical layout. Also, several changes have been made to allow use of CPU boards compatible with the original Altair, rather than requiring the CPU board unique to the 8800b:

STSTB

The 8800b CPU board provides a STSTB~ (S100.56) signal to the front panel. This is used by the front panel to prepare the RDY signal.

The 8800 CPU board does not generate STSTB.

The RIB uses Ø2~ in substitute for STSTB. This 'should' be Ø1 but an attempt to use Ø1 did not provide enough time till Ø2 for the propagation delay of the long string of gates generating RDY.

FRDY

The original 8800 uses pRDY (S100.72) to start/stop the CPU for front panel operations. pRDY is a shared assert-LOW signal open for use by other boards. The Altair 8800 front panel however, rather poorly, uses a totem-pole driver for pRDY rather than an OC driver.

The 8800b uses a private signal for CPU start/stop: FRDY (S100.58).

The RIB reverts to the use of the shared pRDY, but uses a tri-state driver wired for OC operation for the line. The front panel board is altered to remove an inverter to reduce the gate propagation delay. **Due to the STSTB alteration, the logic has only from +edge of Ø1 till the +edge of Ø2 to produce pRDY.**

DIG1

The original 8800 uses 3 signals across the S100 bus from th e front panel to the CPU to inhibit data-input from the bus during front panel operations: RUN, SS & SSWI~ (S100.71,21,53).

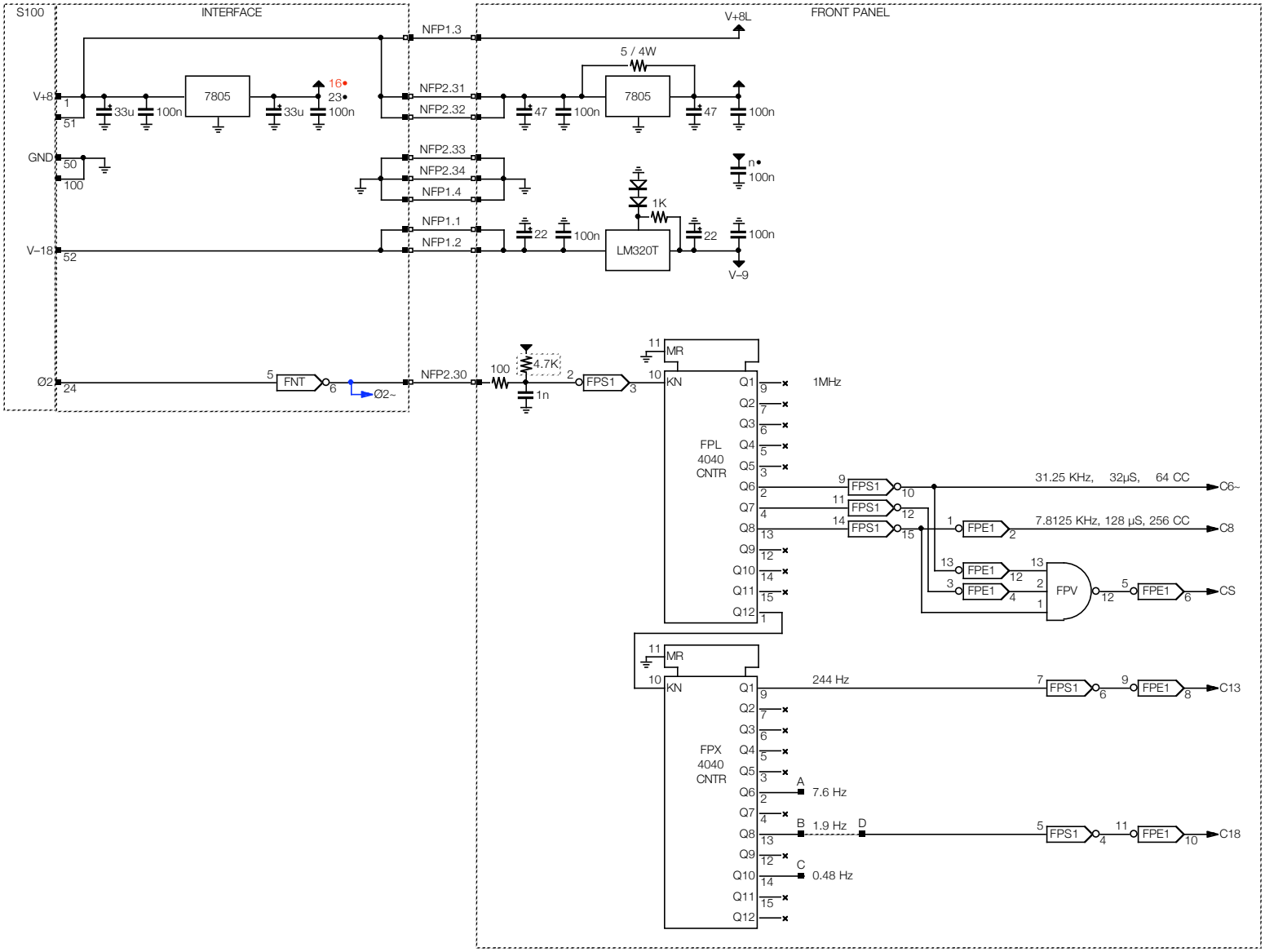
The 8800b uses one signal to this end: DIG1~ (S100.57).

The RIB reroutes DIG1~ to SSWI~.

S S

The Single-Step signal to the 8800 CPU board to permit enabling of the S100 data-input onto the CPU data-bus is not needed. SS (S100.21) sits HIGH by default, permitting said enabling by pDBIN or pHLDA. SSWI~ from the RIB disables S100 data-input whenever the front panel needs to feed data to the CPU (via the CP connector), for sense-switch input or for force-feeding the CPU instructions.

• Note: The 8800b CPU board will not function with the RIB due as presented here, due to the removal of the signals specific to the 8800b.
• Note: The 8800b interface board will not function in a machine modified for the RIB due to the alteration of the RDY output on the front panel board.



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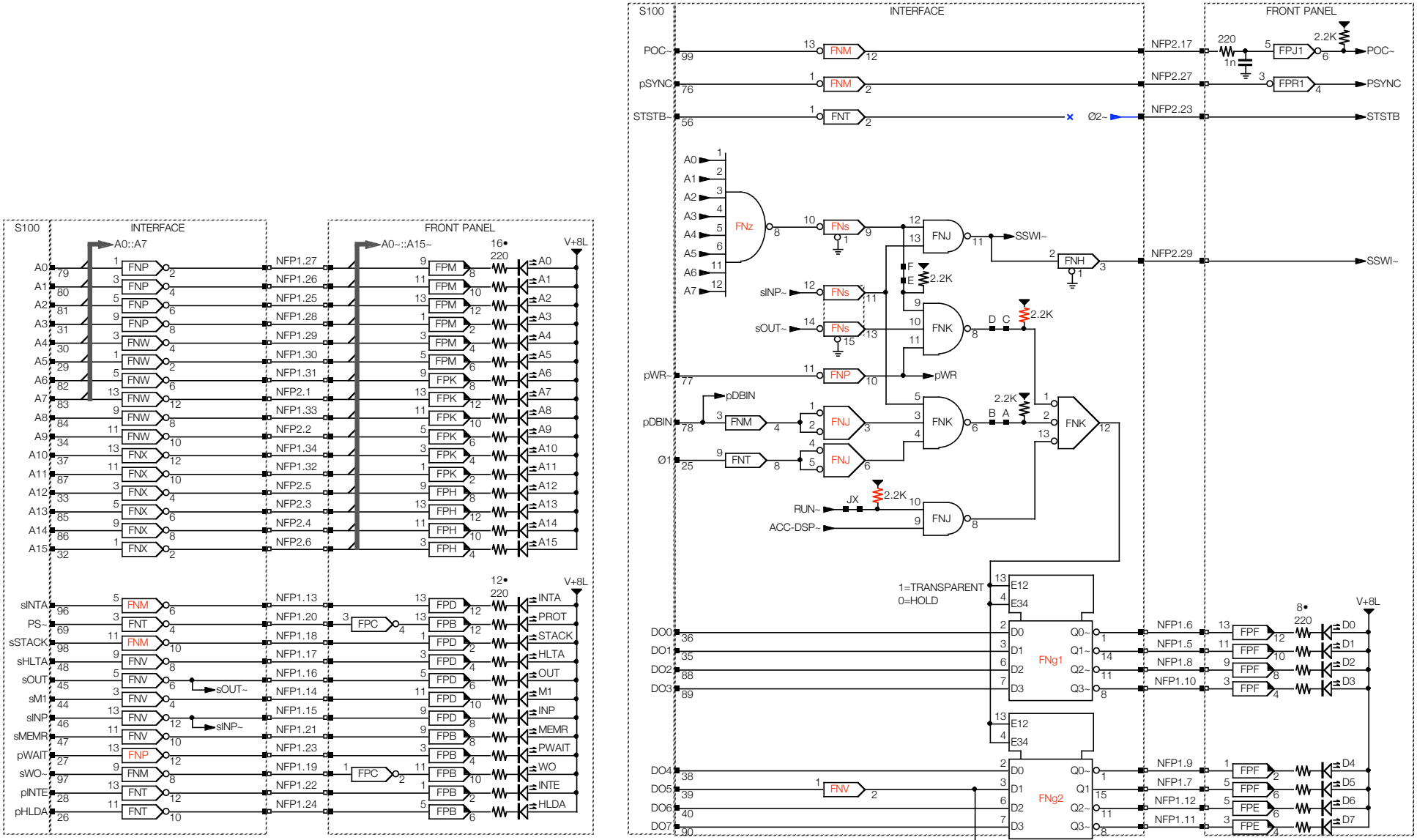
Section: Front Panel - Power & Clock

Page: FP1 Rendition: Mar 8, 2024



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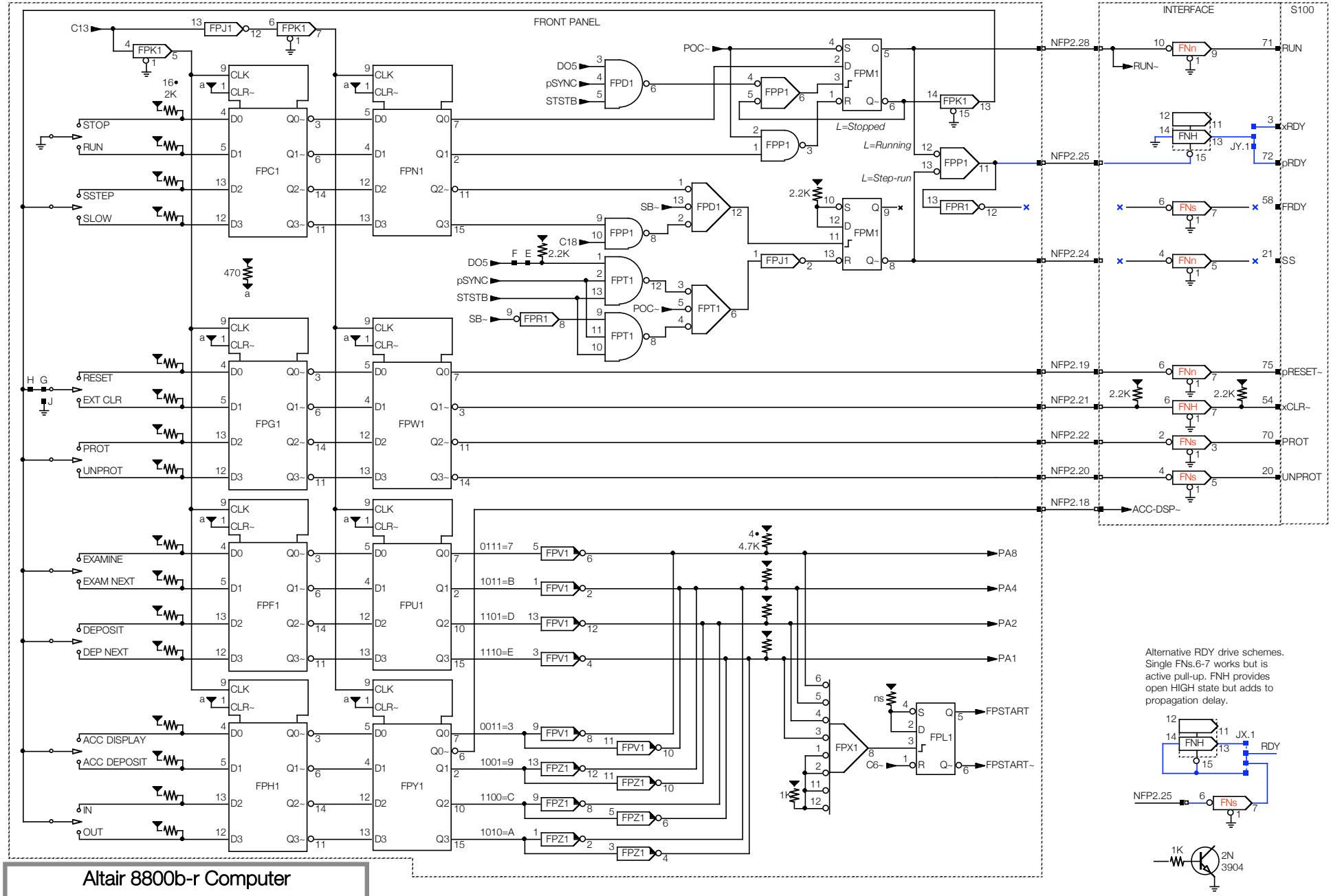
Section: Front Panel - Display LEDs

Page: FP2 Rendition: Mar 8, 2024



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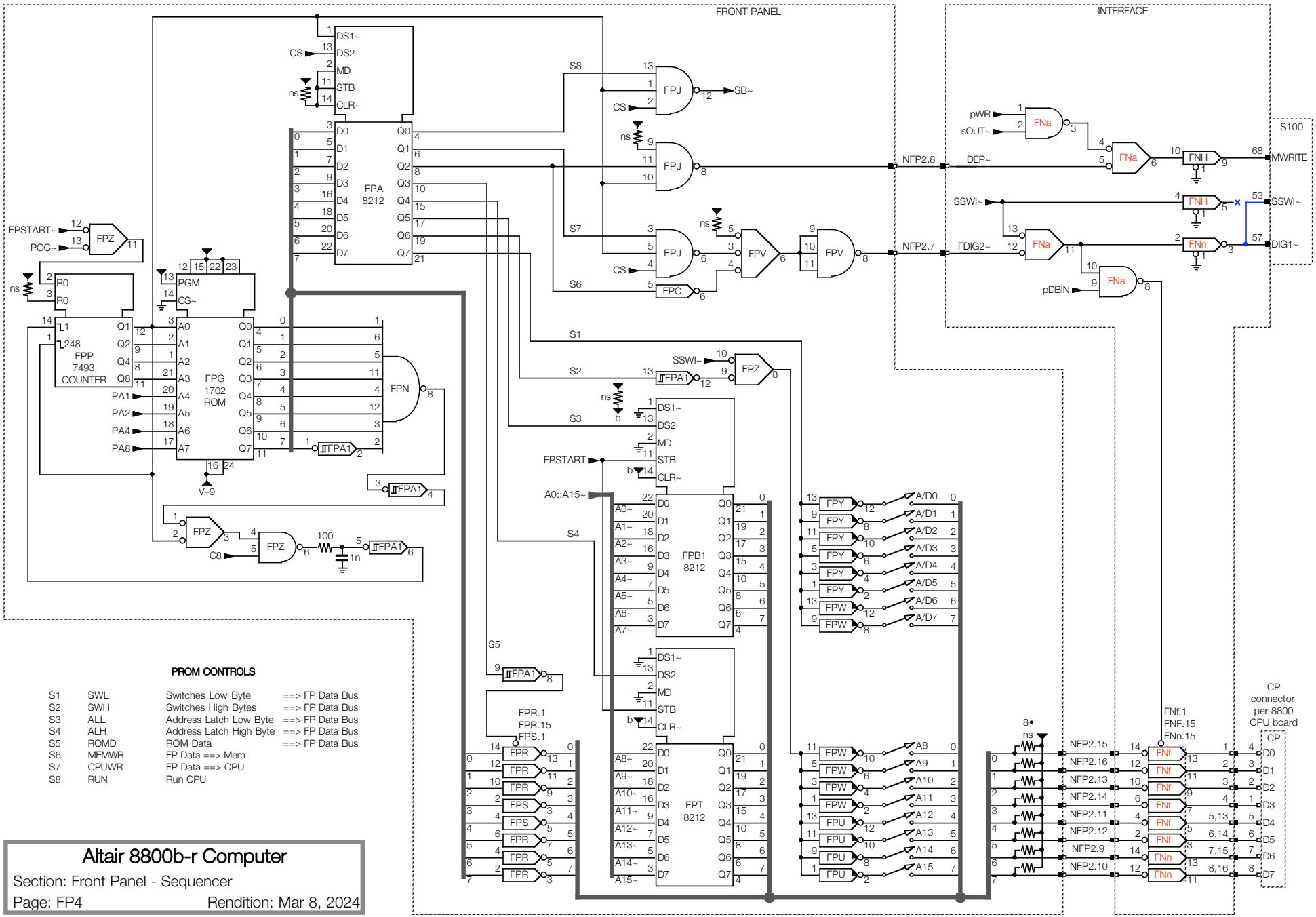
Section: Front Panel - Fct. Switches & Run Control

Page: FP3 Rendition: Mar 8, 2024



PROM CONTROLS

S1	SWL	Switches Low Byte	==> FP Data Bus
S2	SWH	Switches High Bytes	==> FP Data Bus
S3	ALL	Address Latch Low Byte	==> FP Data Bus
S4	ALH	Address Latch High Byte	==> FP Data Bus
S5	ROMD	ROM Data	==> FP Data Bus
S6	MEMWR	FP Data ==> Mem	
S7	CPUWR	FP Data ==> CPU	
S8	RUN	Run CPU	

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Section: Front Panel - Sequencer

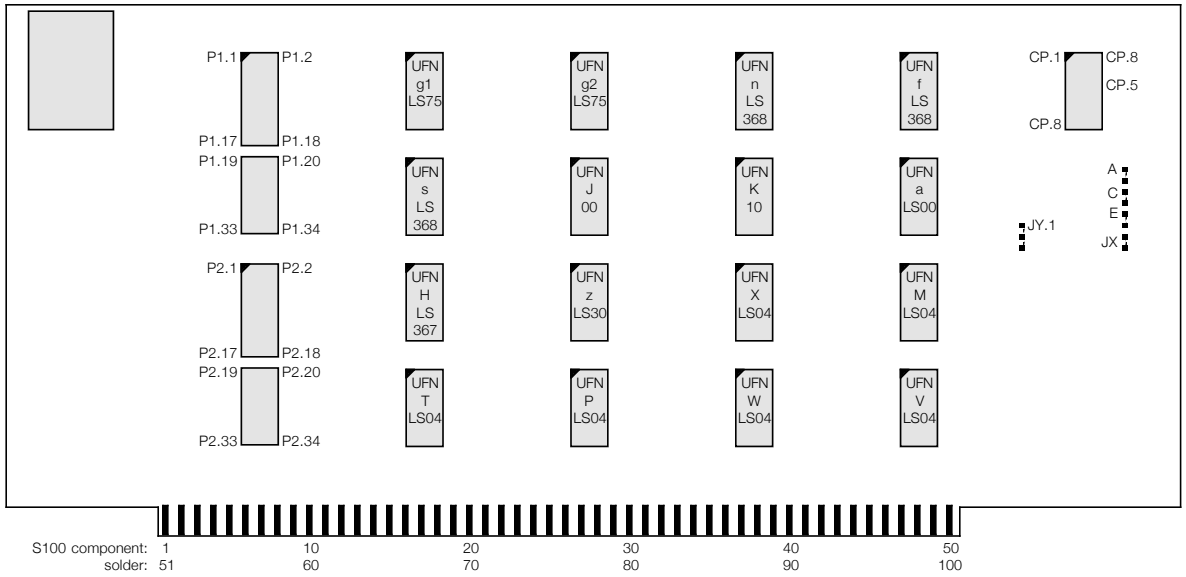
Page: FP4 Rendition: Mar 8, 2024

P1

V–18	1	2	V–18
V+8L	3	4	GND
LD1~	5	6	LD0~
LD5~	7	8	LD2~
LD4~	9	10	LD3~
LD7~	11	12	LD6~
sINTA~	13	14	sMI~
sINP~	15	16	sOUT~
sHLTA~	17	18	sSTACK~
sWO	19	20	PS
MEMR~	21	22	pINTE~
pWAIT~	23	24	pHLDA~
A2~	25	26	A1~
A0~	27	28	A3~
A4~	29	30	A5~
A6~	31	32	A9~
A8~	33	34	A10~

P2

A7~	1	2	A11~
A13~	3	4	A14~
A12~	5	6	A15~
FDIG2~	7	8	**DEP~**
FDI6~	9	10	**FDI7~**
FDI4~	11	12	**FDI5~**
FDI2~	13	14	**FDI3~**
FDI0~	15	16	**FDI1~**
POC	17	18	**ACC-DSP~**
pRESET	19	20	**UNPROTECT~**
xCLR~	21	22	**PROTECT~**
STSTB	23	24	**SS~**
RDY	25	26	DO5~
pSYNC~	27	28	**RUN~**
SSWI~	29	30	Ø2~
V+8	31	32	V+8
GND	33	34	GND



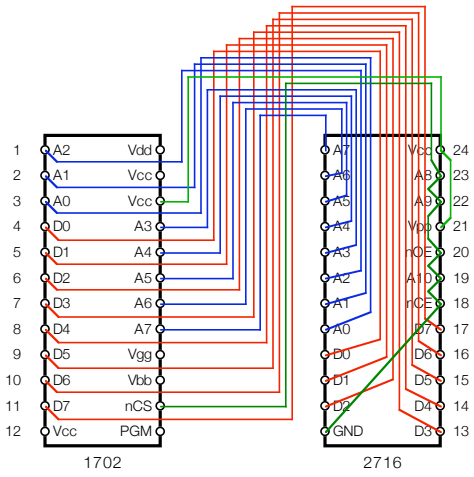
Reconstruction

UFNx	Type	a	b	c	d	e	f
H	74LS367	√	u	√	√	u	s
J	7400	s	s	√	√		
K	7410	s	√	√			
M	74LS04	s	√	√	√	√	s
P	74LS04	√	√	√	√	√	s
T	74LS04	u	√	√	√	√	√
V	74LS04	√	√	√	√	√	√
W	74LS04	√	√	√	√	√	√
X	74LS04	√	√	√	√	√	√
a	74LS00	n	n	n	n		
f	74LS368	n	n	n	n	n	n
n	74LS368	n	u	n	n	n	n
s	74LS368	n	n	u	s	s	s
z	74LS30	n					
g1	74LS75	n					
g2	74LS75	n					

Total ICs: 16

Type	Count	Pins	V+5	GND
7400	1	14	14	7
74LS00	1	14	14	7
74LS04	6	14	14	7
7410	1	14	14	7
74LS30	1	14	14	7
74LS75	2	16	5	12
74LS367	1	16	16	8
74LS368	3	16	16	8
Total:	16			
14 Pin:	10			
16 Pin:	6			

2716 ==> 1702 Adapter



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Section: Front Panel - Interface Recon. Layout & ICs

Page: FP5 Rendition: Mar 8, 2024